# QUAD development

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NIKHEF

Nikhef/Bonn LepCol meeting
October 9, 2017

DAQ and continuation

- Thanks to Bas first electrical QUAD now fully operational using 4 class D chips
- Using Nikhef SPIDR board
- Chips can be addressed, configured, data read out
  - Minor modification on wire bonding scheme
- Temperature reading available
- One resistor to be added to the LV power board
  - Avoiding faulty over-temperature shutdown
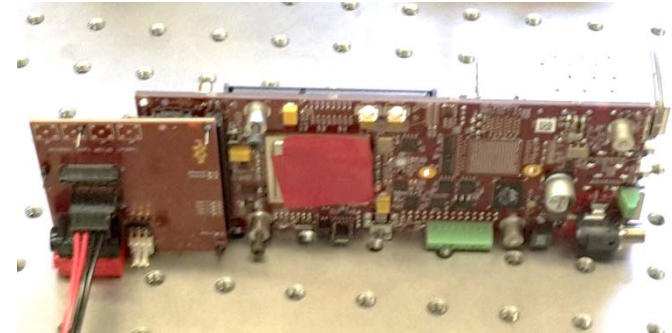
- We may consider ordering soon another five wirebond boards/flexes for the second prototype series
 - After minor modifications
    - Holes for guard screws
    - Modified guard
    - HV board
  - ~15 k €
- Wafers
  - 2 high yield wafers available at Nikhef
  - 2 low yield wafers on the way from CERN to Nikhef
  - All to be sent to Yevgen as soon as they are have arrived at Nikhef

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Next electrical module

- Waiting for chip addresses from Jochen to select acceptable chips
- Alignment of chips easily: within an hour
    - Additional routine to verify the chip position afterwards
- Also wire bonding rapidly (automatic bonder)
- 1 day electrical testing (Bas)
- 3 days for making the HV connection to the grids
    - 3 partly critical glue steps

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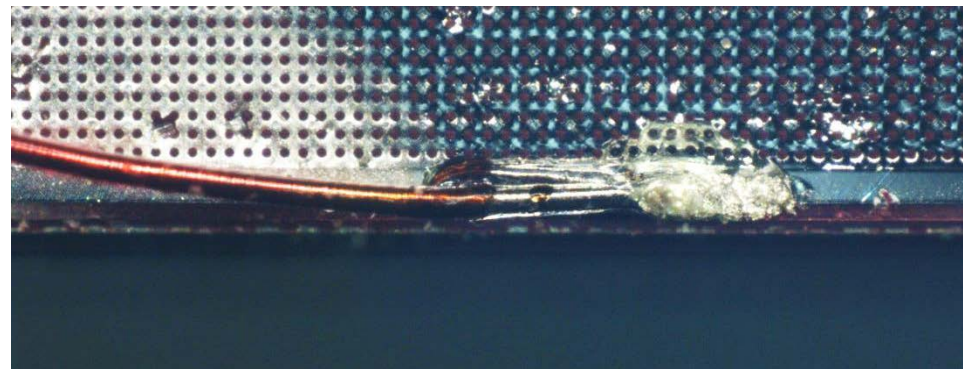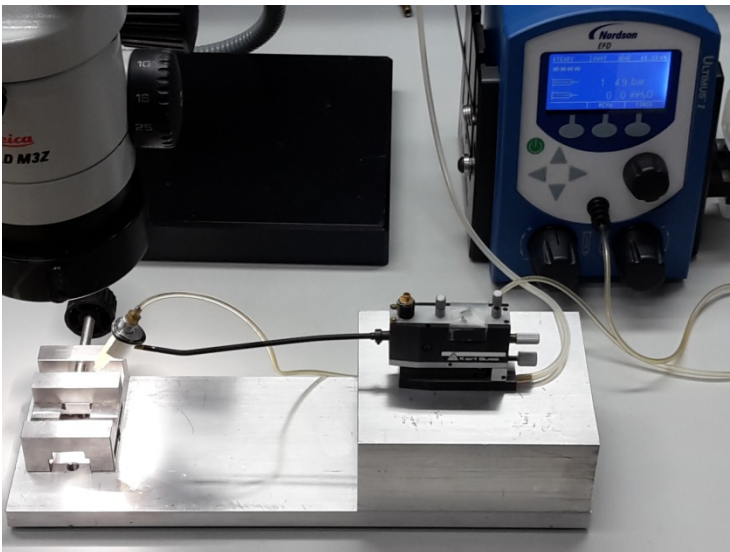
Chip inventory

- 2 class D, reasonable grid
  - H3; G4
  - Both bad: > 35k bad pixels
- Received from Jochen September 27:
  - 6 class A poor grid (wrinkles)
  - 2 class B bit less poor grid
  - 3 class C mediocre grid
  - 8 class D reasonable grid

- How well can we use class D?
  - May have unlimited number of bad pixels
  - Often > 50k
- Whole wafer W15 (105 chips):
  - 28 class D, 11 may be usable
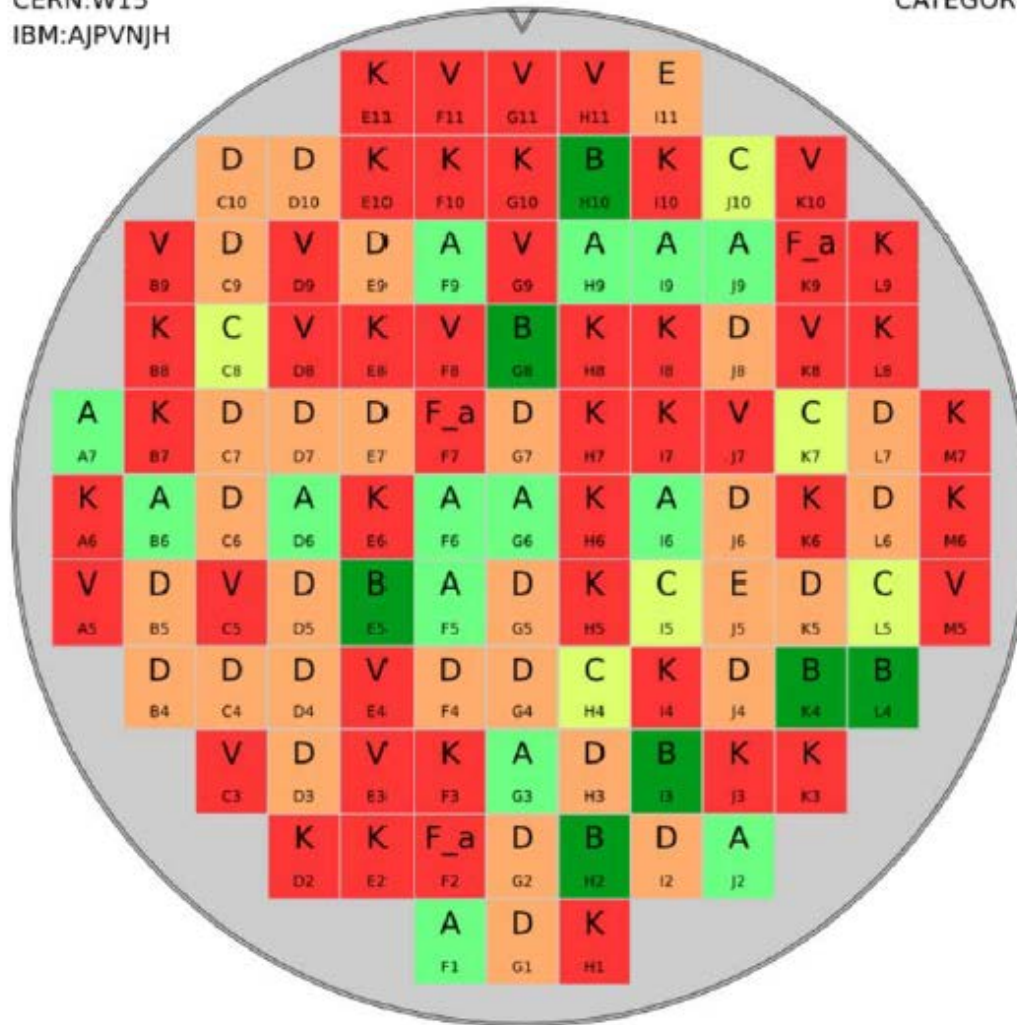- We need at least 8 chips for the next two electrical QUADs + few spares

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Map W15

W15

CERN:W15
IBM:AJPVNJH

CATEGORY

| A [14] | B [7] | C [6] | D [28] | E [2] | F [48] |

Die	Date	Category	Log	Results	Details
W15_A5	2014/12/05 18:44:31	V	37.0 KB	3.1 KB	28.3 KB
W15_A6	2014/12/05 18:44:11	K	57.4 KB	3.1 KB	34.9 KB
W15_A7	2014/12/05 17:44:15	A	67.6 KB	4.4 KB	1.2 MB
W15_B4	2014/12/05 19:50:09	D	364.3 KB	4.3 KB	967.2 KB
W15_B5	2014/12/05 18:44:45	D	857.9 KB	4.3 KB	920.2 KB
W15_B6	2014/12/05 18:40:21	A	59.7 KB	4.4 KB	1.2 MB
W15_B7	2014/12/05 17:47:40	K	57.0 KB	3.1 KB	35.8 KB
W15_B8	2014/12/05 17:43:55	K	62.1 KB	3.1 KB	38.4 KB
W15_B9	2014/12/05 17:04:48	V	36.7 KB	3.1 KB	28.0 KB
W15_C10	2014/12/05 17:00:43	D	999.5 KB	4.3 KB	908.6 KB
W15_C3	2014/12/05 19:53:30	V	36.9 KB	3.1 KB	28.2 KB
W15_C4	2014/12/05 19:46:19	D	65.1 KB	4.4 KB	1.2 MB
W15_C5	2014/12/05 18:47:58	V	36.9 KB	3.1 KB	28.2 KB
W15_C6	2014/12/05 18:36:27	D	94.4 KB	4.4 KB	1.2 MB
W15_C7	2014/12/05 17:48:00	D	858.2 KB	4.3 KB	880.3 KB
W15_C8	2014/12/05 17:40:05	C	59.0 KB	4.4 KB	1.2 MB
W15_C9	2014/12/05 17:05:02	D	941.4 KB	4.3 KB	294.5 KB
W15_D10	2014/12/05 16:56:51	D	81.1 KB	4.4 KB	1.2 MB
W15_D2	2014/12/05 20:28:27	K	64.0 KB	3.1 KB	36.3 KB
W15_D3	2014/12/05 19:53:43	D	78.1 KB	4.4 KB	1.2 MB
W15_D4	2014/12/05 19:42:49	D	894.2 KB	4.3 KB	894.8 KB
W15_D5	2014/12/05 18:48:11	D	192.3 KB	4.4 KB	1.2 MB
W15_D6	2014/12/05 18:32:42	A	59.0 KB	4.4 KB	1.2 MB
W15_D7	2014/12/05 17:51:09	D	80.4 KB	4.4 KB	1.2 MB
W15_D8	2014/12/05 17:39:51	V	36.5 KB	3.1 KB	28.1 KB
W15_D9	2014/12/05 17:08:26	V	36.7 KB	3.1 KB	28.5 KB
W15_E10	2014/12/05 16:56:32	K	52.6 KB	3.1 KB	35.4 KB
W15_E11	2014/12/05 16:31:26	R	4.9 KB	119.0 B	2.5 KB
W15_E11	2014/12/05 16:43:15	K	247.9 KB	3.1 KB	50.3 KB
W15_E2	2014/12/05 20:28:07	K	62.6 KB	3.1 KB	35.7 KB
W15_E3	2014/12/05 19:57:34	V	36.7 KB	3.1 KB	28.4 KB
W15_E4	2014/12/05 19:42:35	V	36.7 KB	3.1 KB	28.1 KB
W15_E5	2014/12/05 18:51:59	B	61.5 KB	4.4 KB	1.2 MB
W15_E6	2014/12/05 18:32:23	K	62.0 KB	3.1 KB	34.7 KB
W15_E7	2014/12/05 17:55:02	D	321.0 KB	4.3 KB	933.0 KB

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Class D chips

- > 1024 bad pixels, no upper limit
- "good" class D chips (11 out of 28)
  - Few hundred randomly situated dead pixels
  - Few dead columns
  - Example: chip D3
    - Bad pixels: 291
    - Bad columns: 2
    - Bad super pixels: 31
    - Log file: 78.1 k
- "bad" class D chips (17, easily selected by size of the log file)
  - 50 k – 64 k bad pixels (practically all pixels are bad)
  - Example: Chip D4
    - Bad pixels: 49564
    - Bad columns: 256
    - Bad super pixels: 8147
    - Log file 894.2 k

Chip C4

```
[226969] Final categorization
[226973]    Found 256 bad pixels in column 192
[226974]    Found 13 bad pixels in column 230
[226974]    Found 12 bad pixels in column 231
[226985]    Found 8 bad pixels in super pixel dc=115 sp=53
[226985]    Found 8 bad pixels in super pixel dc=115 sp=54
[226985]    Found 8 bad pixels in super pixel dc=115 sp=55
[226987] Bad pixels : 307
[226987] Bad columns : 3
[226987] Bad super pixels : 3
[226987] Chip category D
```

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Metrology

- Results so far using a dummy chip (class E)
- Using verification routine afterwards
- We refer to the bonding pads
  - Grid presently not sufficiently reliable (wrinkles)
- Error in X: ~10 µm
  - Partly systematic by pressing the chip on the double sticky tape
  - We may anticipate on this
- Error in Y: normally 0 – 3 µm
  - measuring error of microscope system
- Errors stable for several days
  - No sign of creep

- But alignment is done using **two** reference corners for only **two** chips at a time
 - We depend on the real dimensions of the COCA

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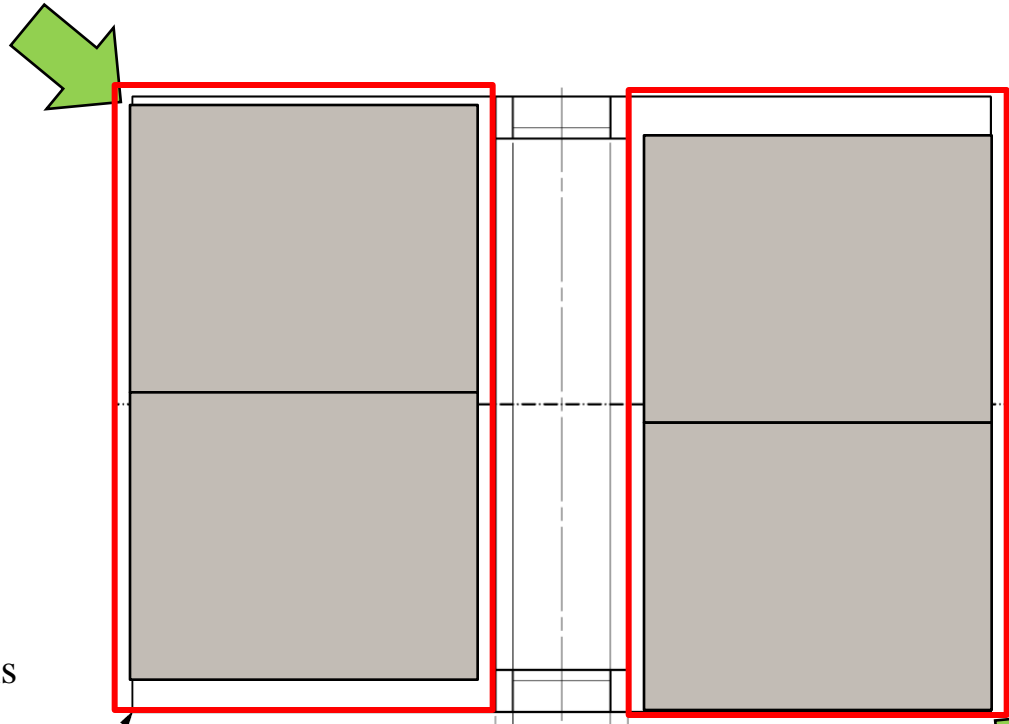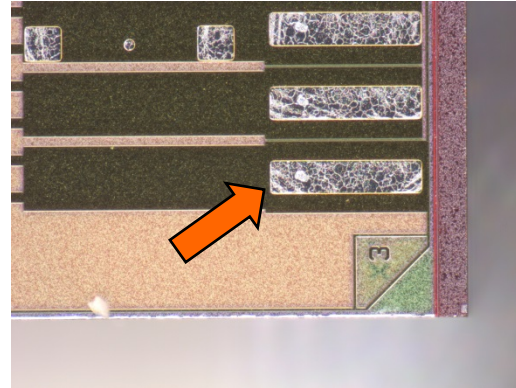
Metrology (cntd)

- We will compensate an error due to wrong COCA dimensions

  - Adapting the chip positions to COCA dimension

  - We have a screw micro meter to measure the COCA dimensions to µm resolution

  - Doing the verification on all **four** chips in one go

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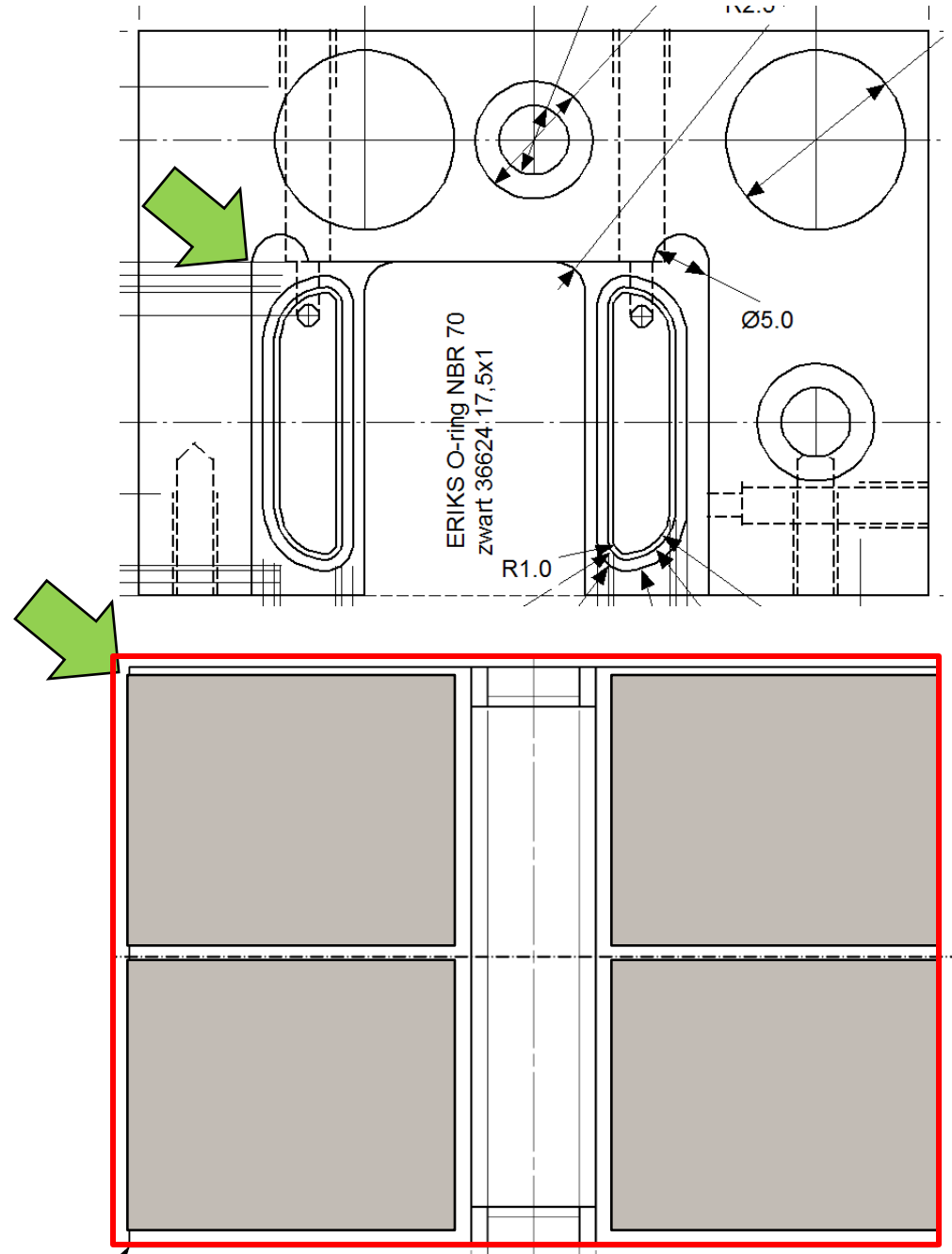
QUAD test box

- All parts fabricated
- Assembly almost finished
  - Commissioning starting soon
- Expected to be operational this week
- One laser window on the front
- Two Kapton windows on the sides
- Laser scan volume 50 x 50 x 25 mm (X, Y, Z)
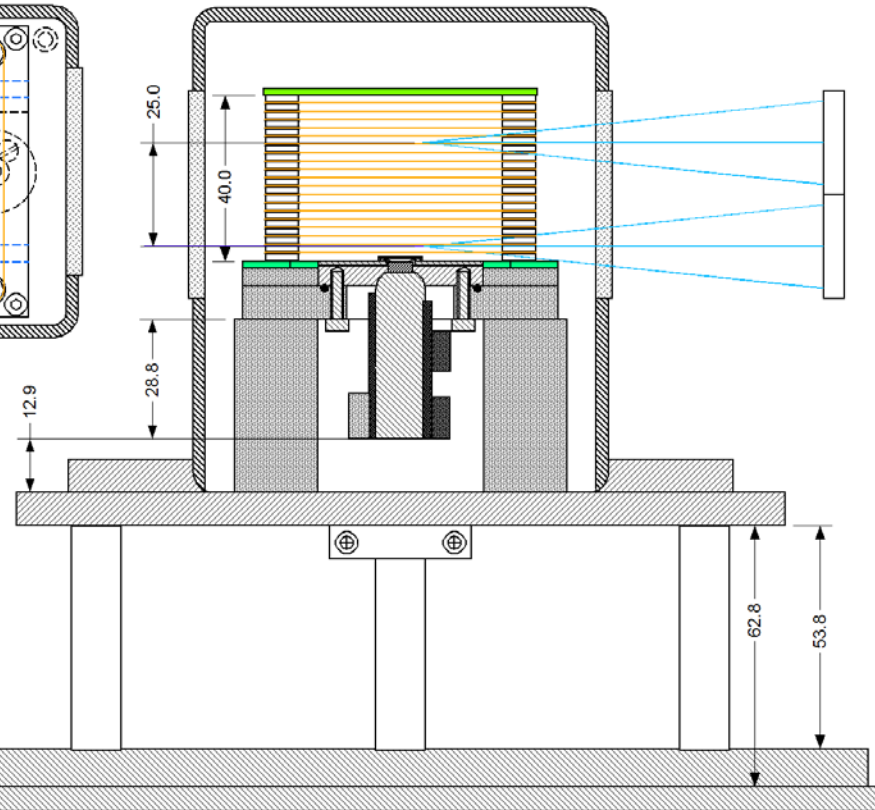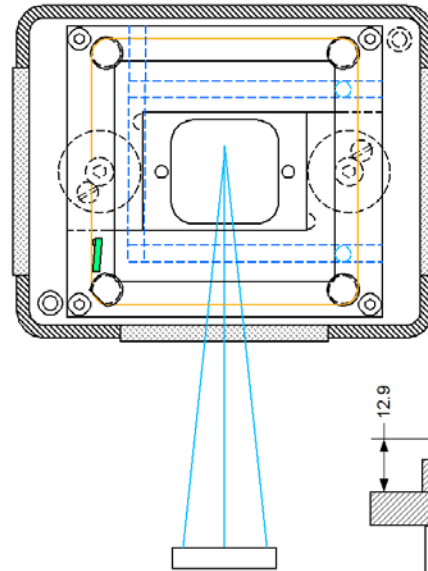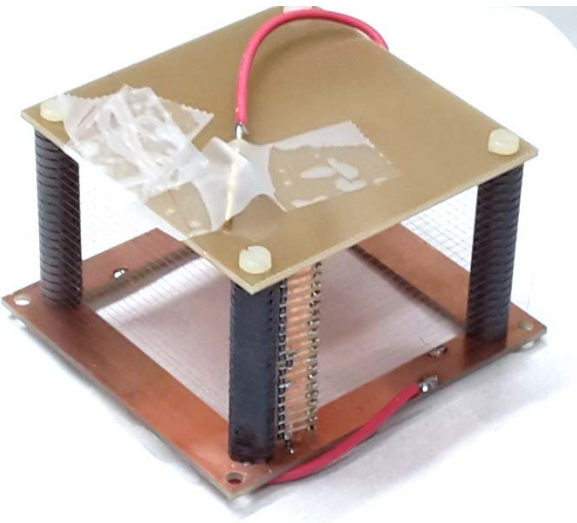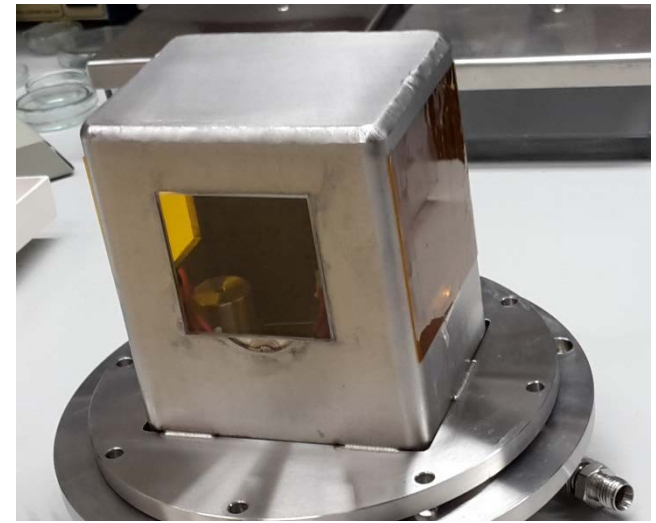
Summary

- Electrical QUAD 2 to be finished in ~1 week
- Testbox including installation and commissioning to be finished in ~1 week
  - First starting with laser measurements
  - Later to test beam (Bonn?)
- Who will run the laser setup, do the analysis?

- We have to work out further issues
  - Metrology
    - References in X, Y and Z
  - Create a data base with metrology results

- New PCBs have to be ordered after minor modifications

- Shortage of good chips with InGrid
  - We can only use mediocre chips for next two QUADs
  - We should start new InGrid production using the two low yield and two high yield wafers
    - Modified grid

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