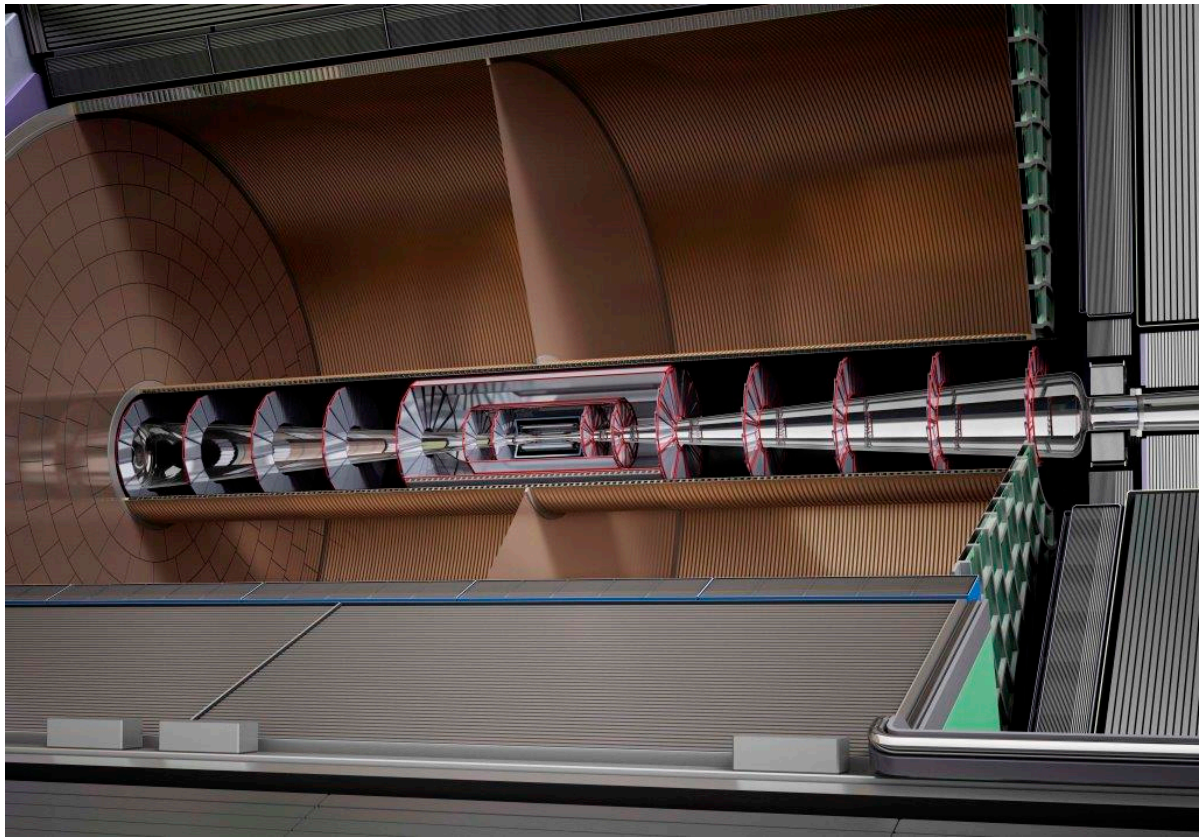
Pixel TPC tiling for ILD



Peter Kluit - Nikhef 11 september 2017

Tiling of the TPC read-out

Basic building block is the quad
- width 28.4 mm height = 39.6 mm
Sensitive area width and height 2 x 256 x 0.055 mm

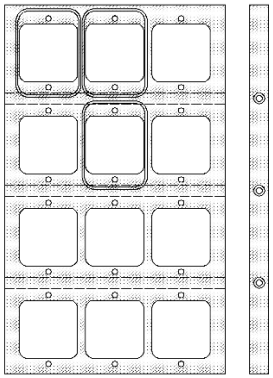
New TPC dimensions Rin = 354 mm Rout = 1768.8-55 mm

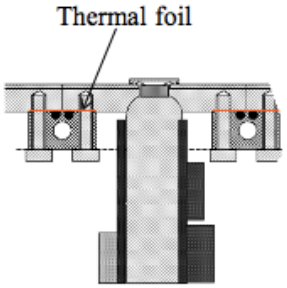
Nr. Of Modules in 8 (radial) rows 14, 18, 23, 28, 32, 37, 42, 46

Tiling of the TPC read-out

Solving the maximum number of quads per quad row number in the module. Putting the quads on a straight line:

Row 8	8 7 7 7 (8 large radius)
Row 5,6,7	7 7 7 7
Row 4 ,3	7 7 7 6
Row 2	7 7 6 6
Row 1	7 6 6 5





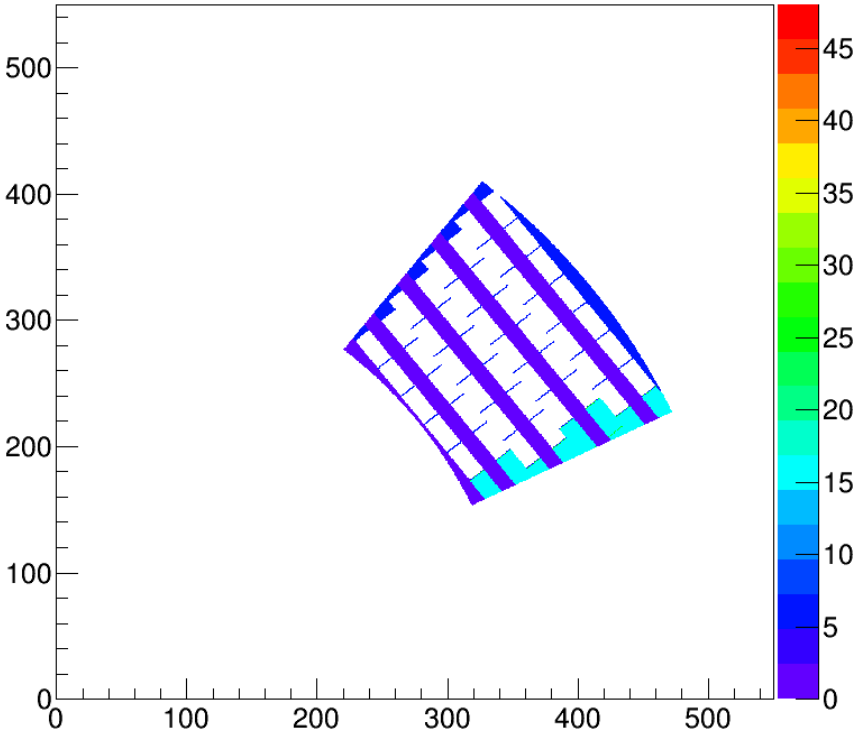
Most simple solution is just start tiling on the left side and leave uncovered space at the module edges.

Another solution – suggested by Jan - is to leave no space at the edges and allow space between quad nr 6-5 nr 5-4 nr 4-3 nr 3-2 (quadrow bottom to top). This avoids an insensitive zone at the edge of a module.

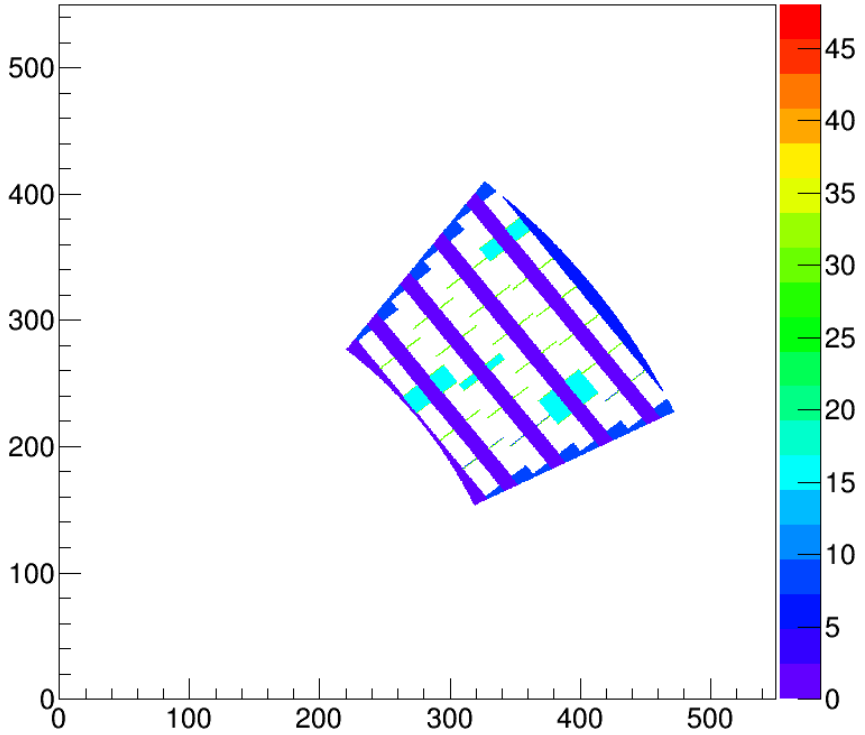
Tiling of the TPC read-out

Example of module most inner row

Simple solution



Complex solution



In dark blue Module edges
Light blue empty space (in between/edge)
Green between two quads
Purple inside quad (guard above wirebonds)

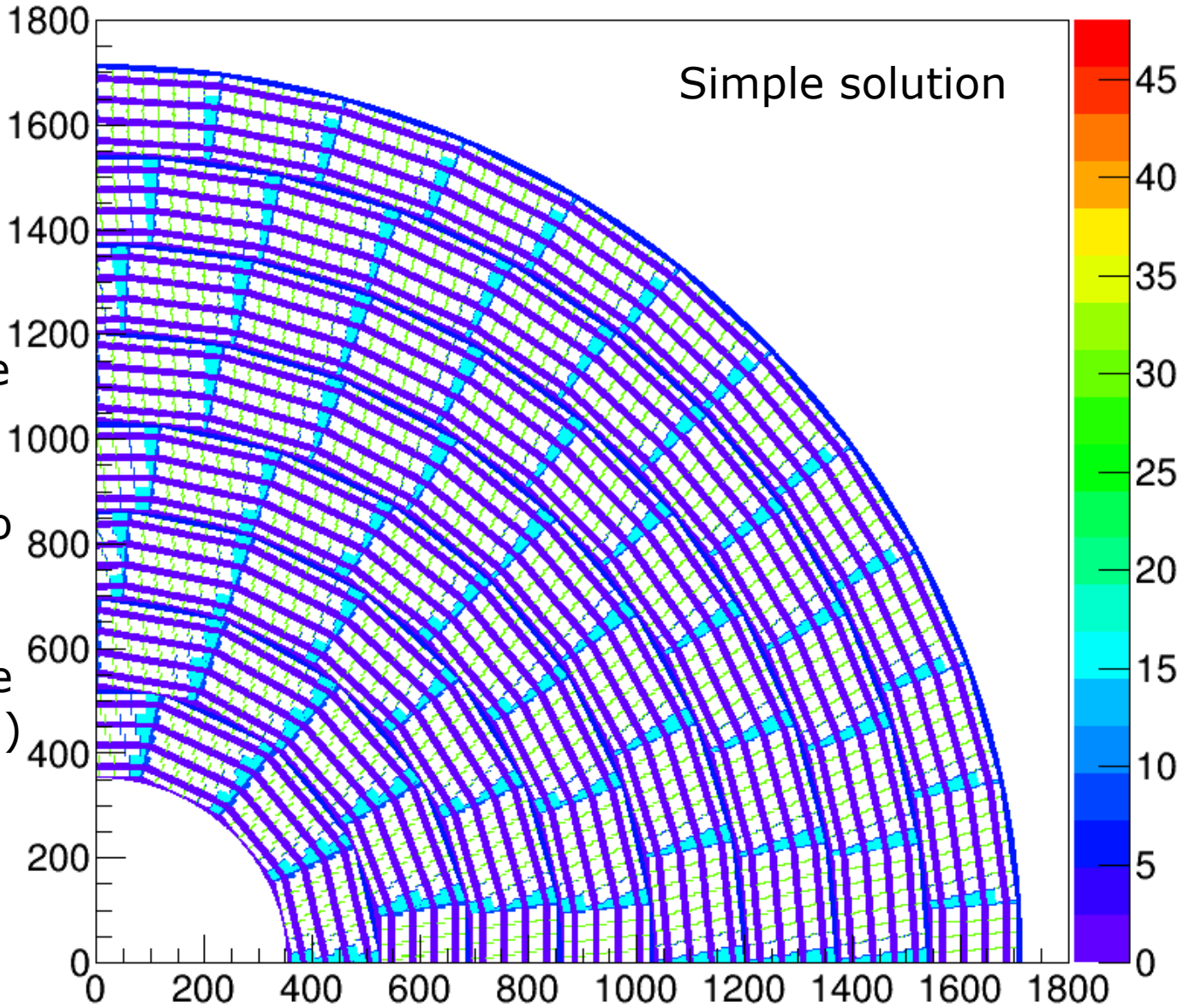
Tiling of the TPC read-out

Insensitive areas

In light blue Module edge

Green between two quads

Purple inside quad (guard)



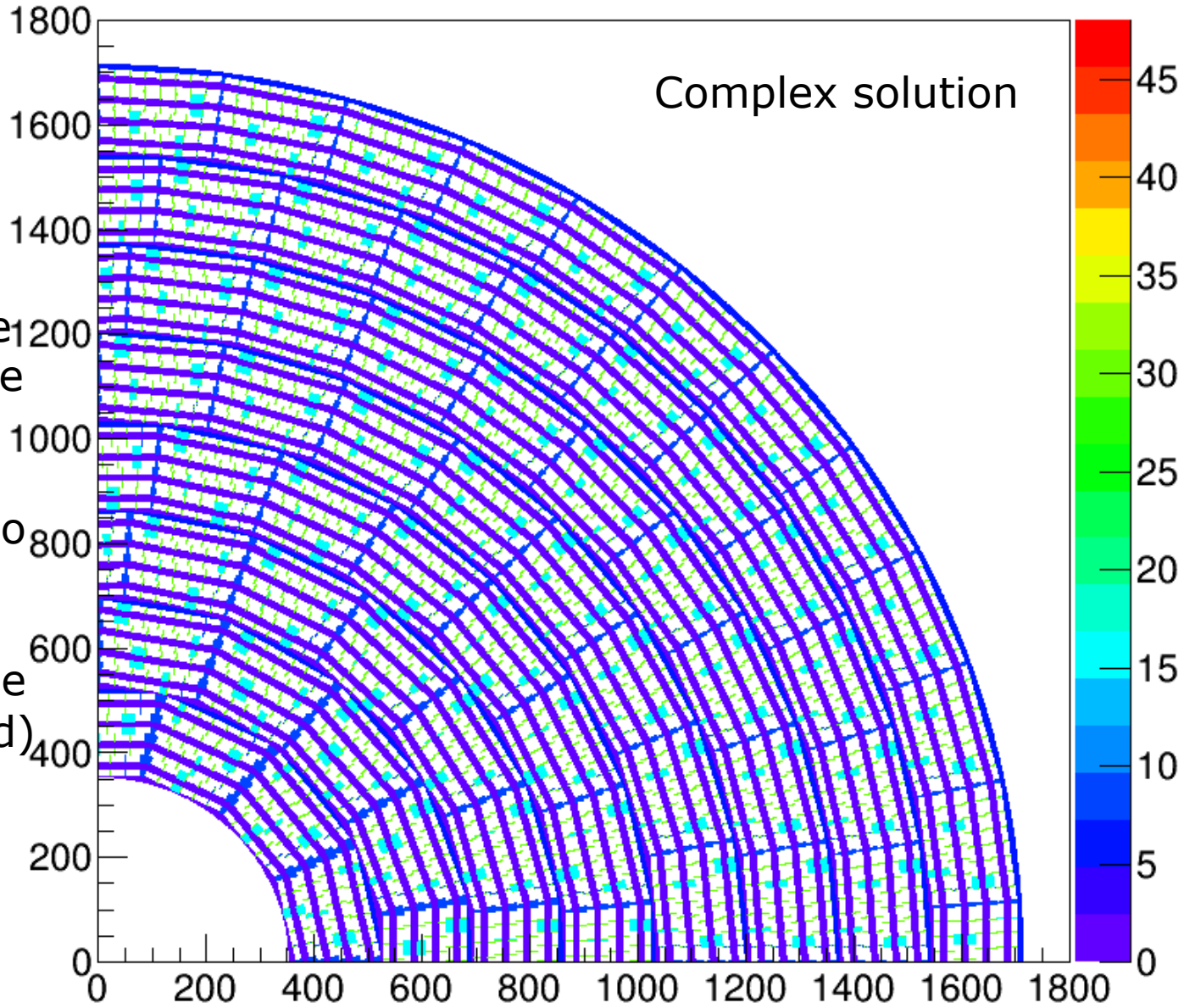
Tiling of the TPC read-out

Insensitive areas

In light blue Module edge

Green between two quads

Purple inside quad (guard)

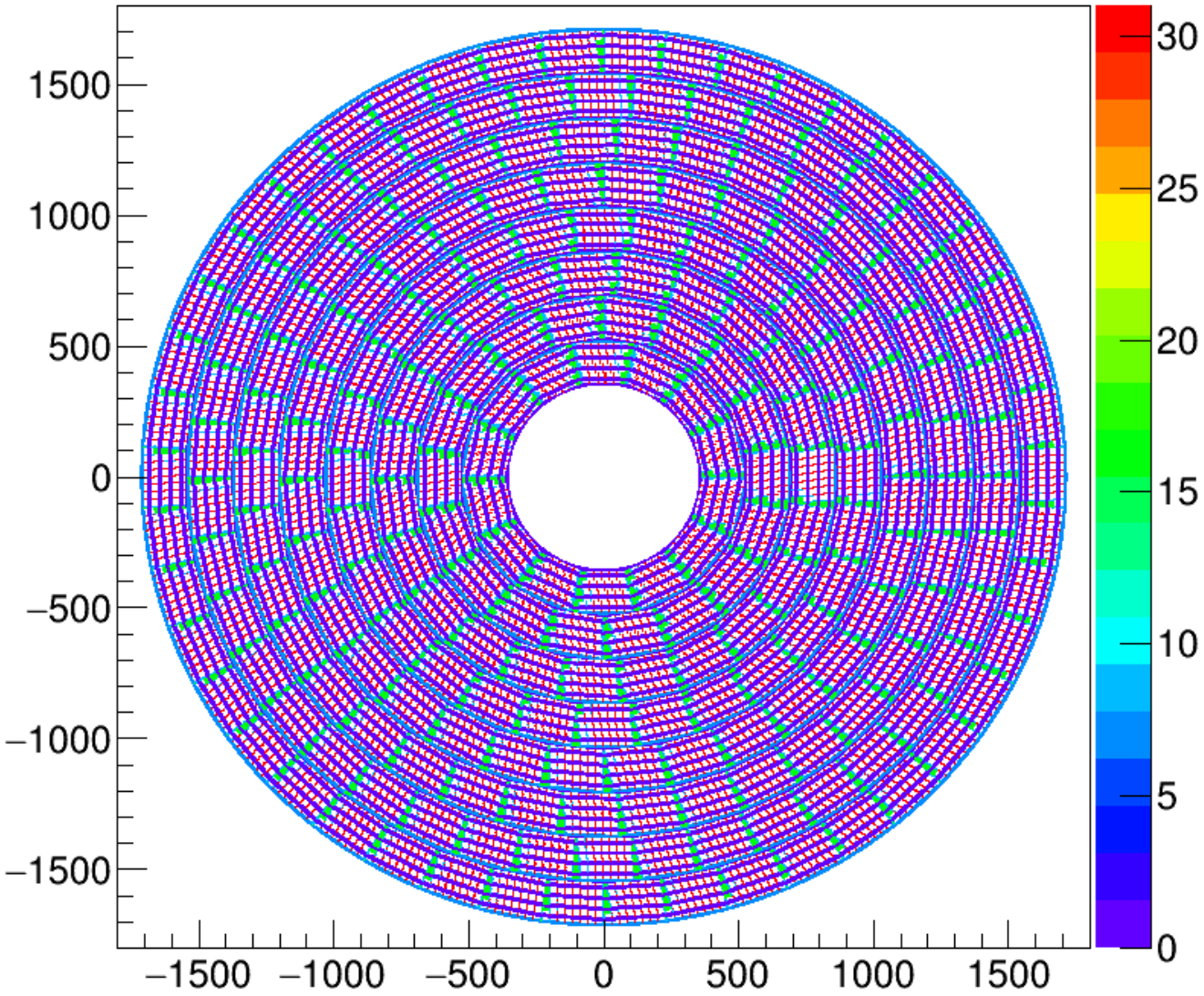


Tiling of the TPC read-out

Simple solution

Insensitive areas

In light blue Module edge

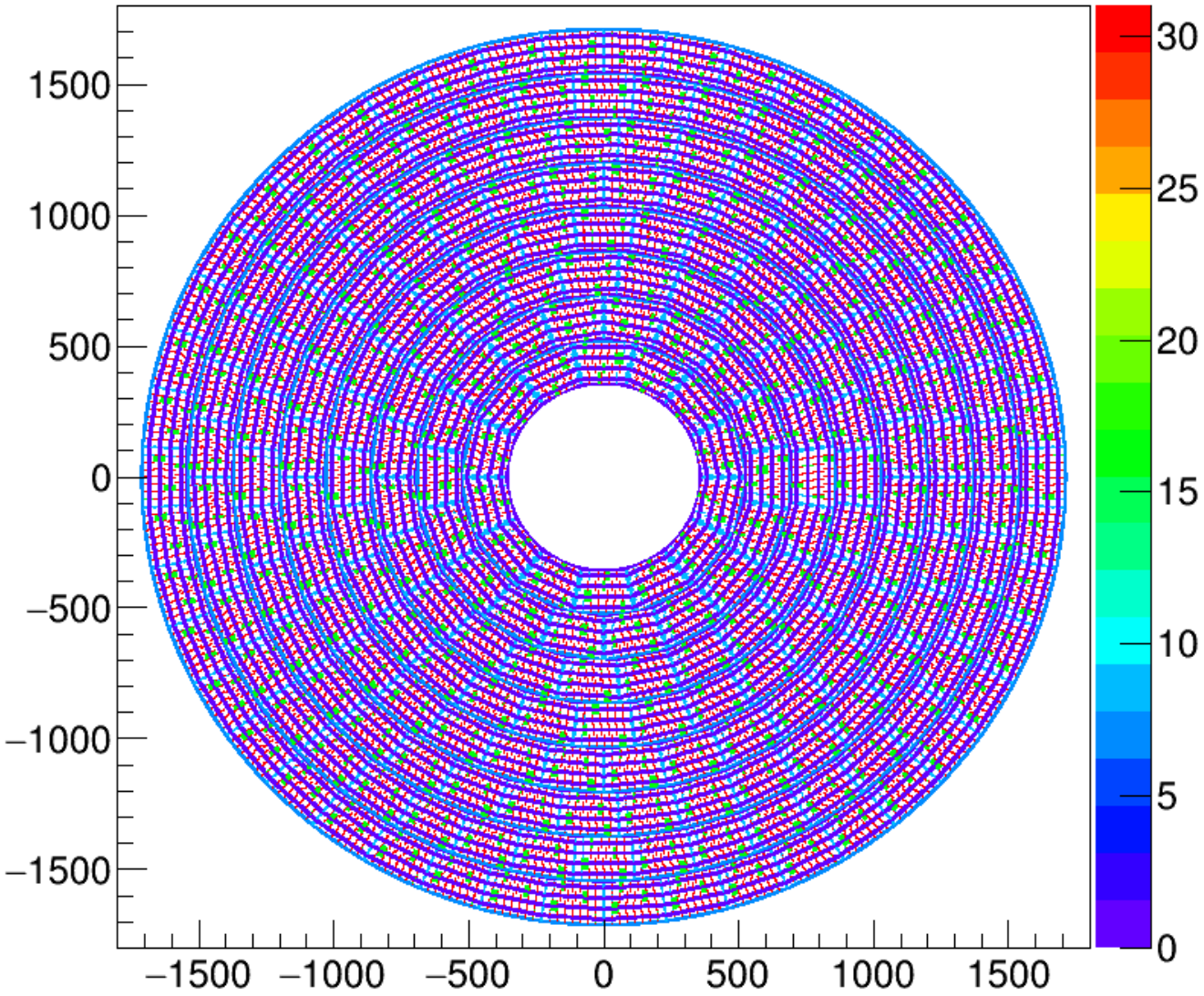


Tiling of the TPC read-out

Complex solution

Insensitive areas

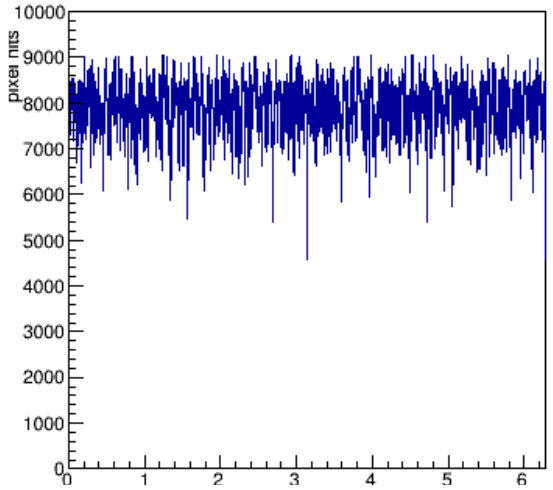
In light blue Module edge

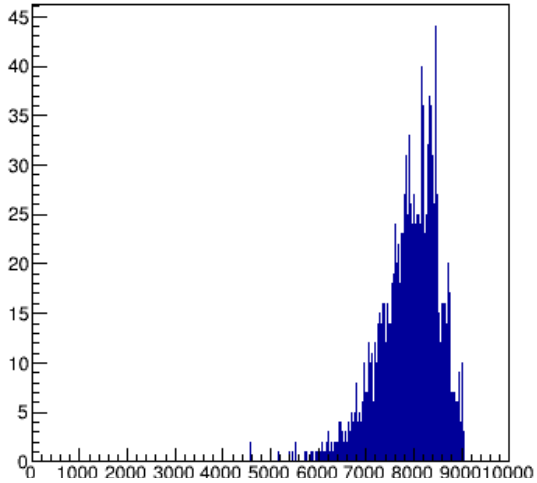


Tiling of the TPC read-out

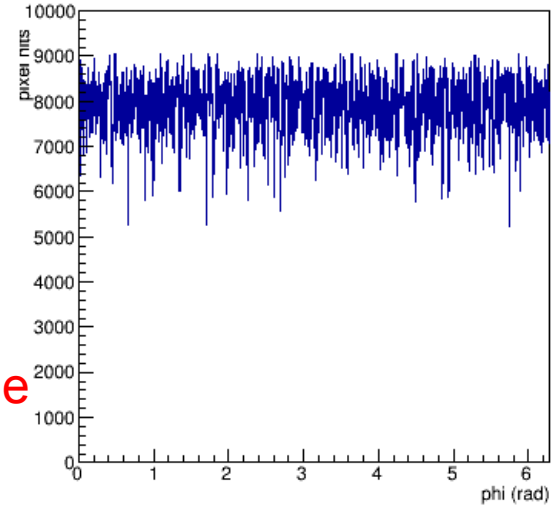
Complex solution hits per track

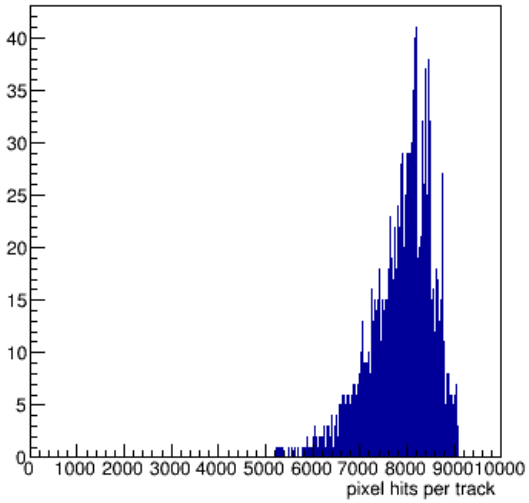
Staggered geometry





Phi module rotating vs row





Better phi coverage

Summary: Tiling of the TPC read-out

Quad surface 1124.64 mm^2
Quad coverage 0.696839

Total quads 6623
Total quad sensitive surface 5.1904e+06 mm^2
Total read-out surface 8.84428e+06 mm^2
Total read-out plane coverage 0.586865

-Most of the coverage loss (30%) is due to the "guard" board between the chip pairs. This board covers the TPX3 chip wire bonding pads.
- Only a relative 15% loss is due to the rectangular tiling on a cylindrical disc.
- Note that some optimization can be done by adjusting the module height and the nr of modules per row.
- Best solution – avoiding aligned dead zones - is the complex tiling
- This layout describes a realistic TPX3 pixel read-out of the TPC that includes all the dead space that can be 1-1 compared to a pad read-out plane (that also now includes dead space).