QUAD development

Fred Hartjes
NIKHEF

Nikhef/Bonn LepCol meeting
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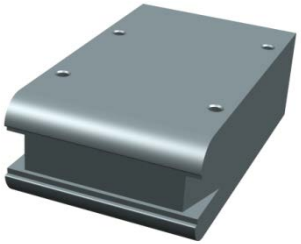
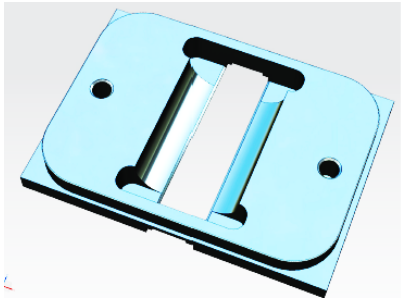
First electrical QUAD (QUAD 1)

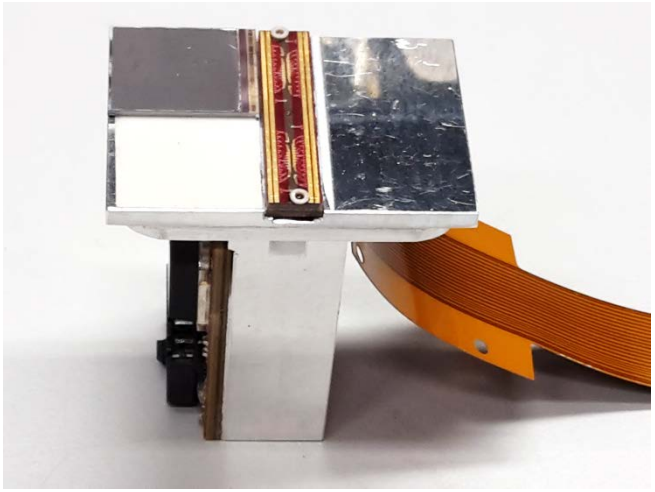
- QUAD 1 being tested
  - Chips show sign of life
  - But DAQ configuration still going on by Bas
- Error found
  - 3 bonds to a termination pin have to be rerouted from VCC to GND
- We need confirmation of proper functioning before ordering a second batch (~15k €)

QUAD 2

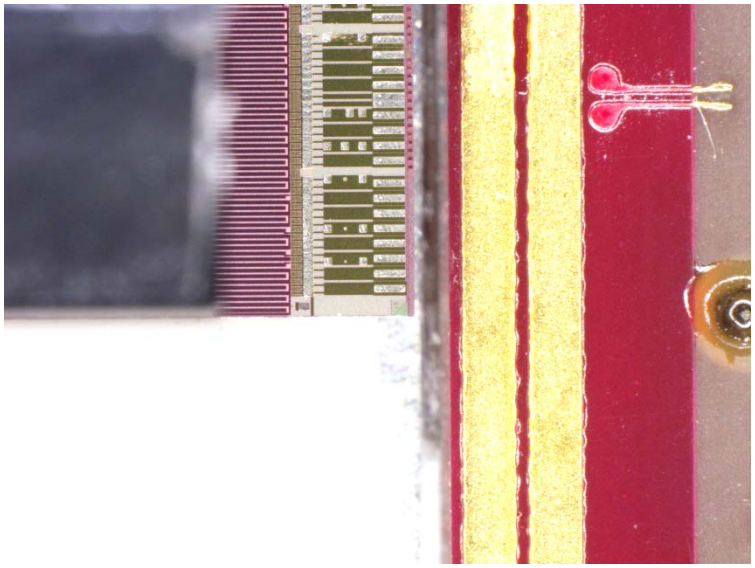




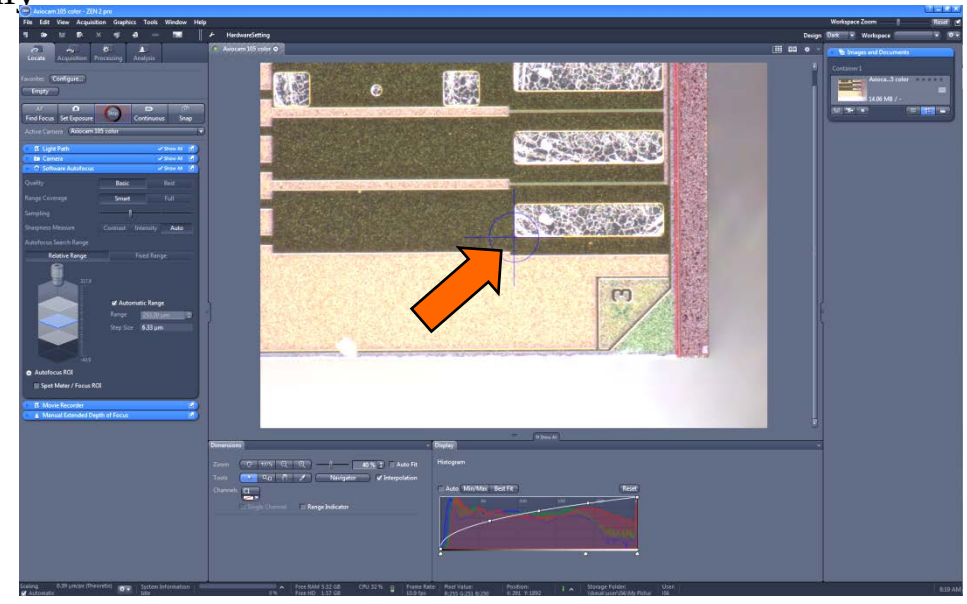
- Coca and stump fabricated to latest modifications
- QUAD 2 glued together using jig
  - Still stump few degrees off
- We have bought surgical microscope to avoid damage when machining wirebond PCB
- Coca surface well cleaned
- Positioning tests with class E chip
  - Wrinkled grid
- Chip is first aligned at ~300 µm above the thermal tape
- Only minor error in XY position after pushing the chip onto the tape
  - Chip does not move anymore when touching it
- Whole alignment procedure is going smoothly now



Chip position in XY

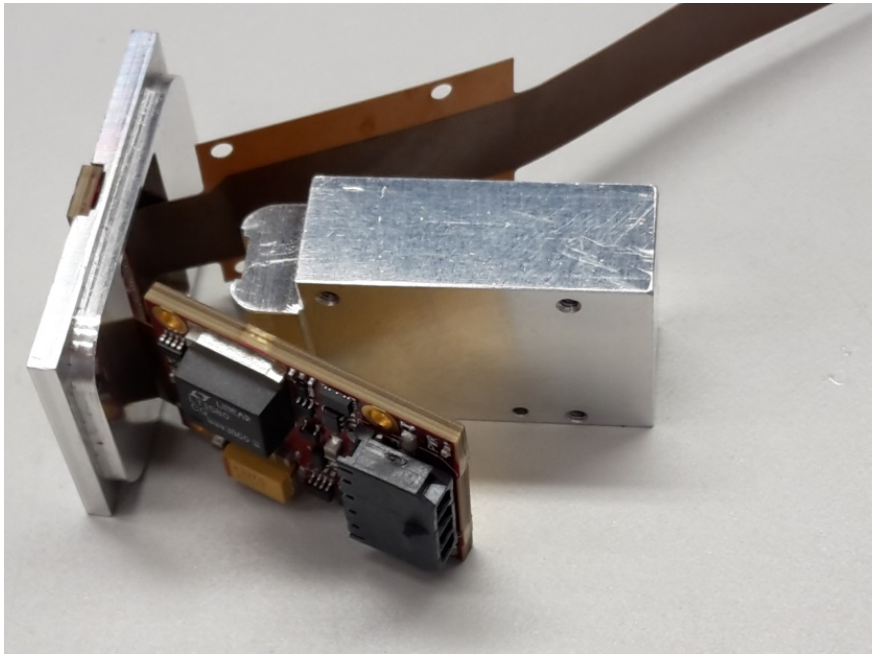


- Preliminary verified
  - 1st bonding pad: $\Delta X = 3.6$ µm, $\Delta Y = 1.4$ µm
  - 2nd bonding pad: $\Delta X = 2.9$ µm, $\Delta Y = 8.0$ µm??
- Dedicated metrology program in progress
- Fine tuning of the chip XY position parameters
  - Nominal distance of chip edge to coca edge: 13 µm
  - Hard to detect precisely the edge of the coca
  - Edge looks quite rough under the microscope
- Chips held very tight by the thermal tape
  - First chip broke when trying to remove it
  - But using some alcohol it went smoothly



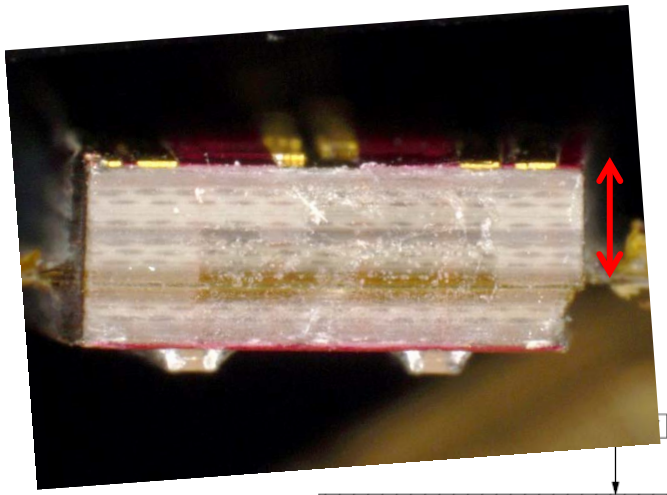
Chip position in Z

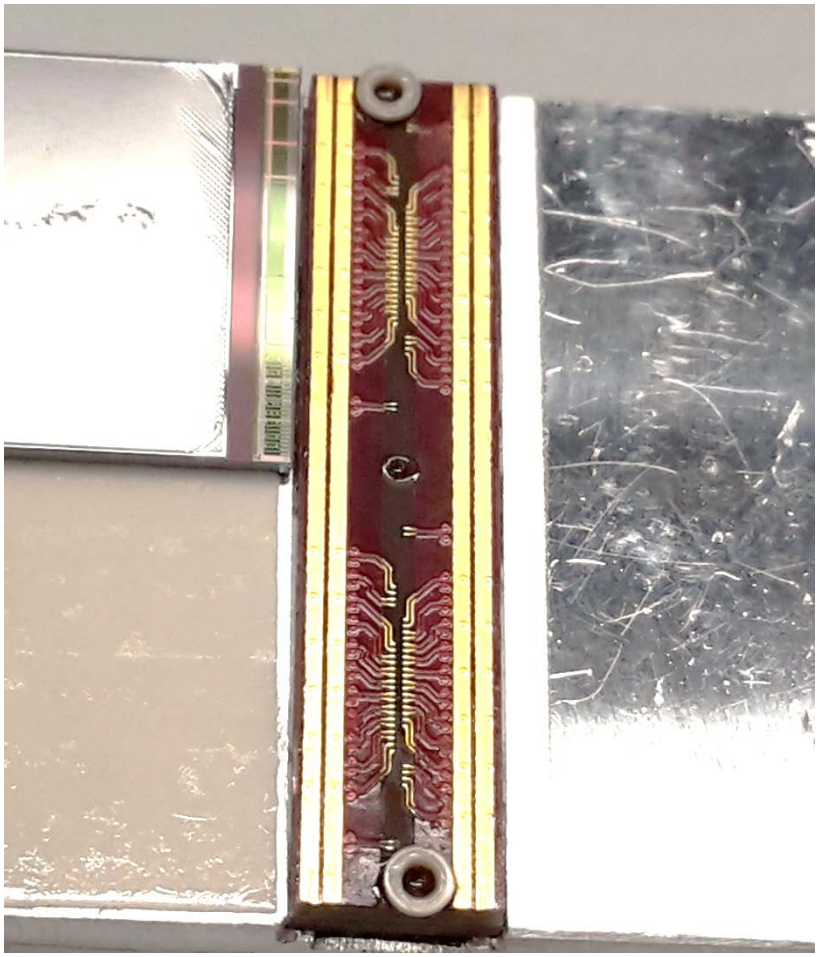
- We use as reference the underside of the coca
  - Coca thickness (4.8 mm) quite well
  - +/- 20 µm
- Z of chip was preliminary verified
  - Within specs along the bonding pads
  - But 30 µm higher at the opposite side
  - Coca does likewise
  - Both coca halves only weakly connected
  - May be pushed upwards by the flexes
  - Could be improved when mounted on support plate

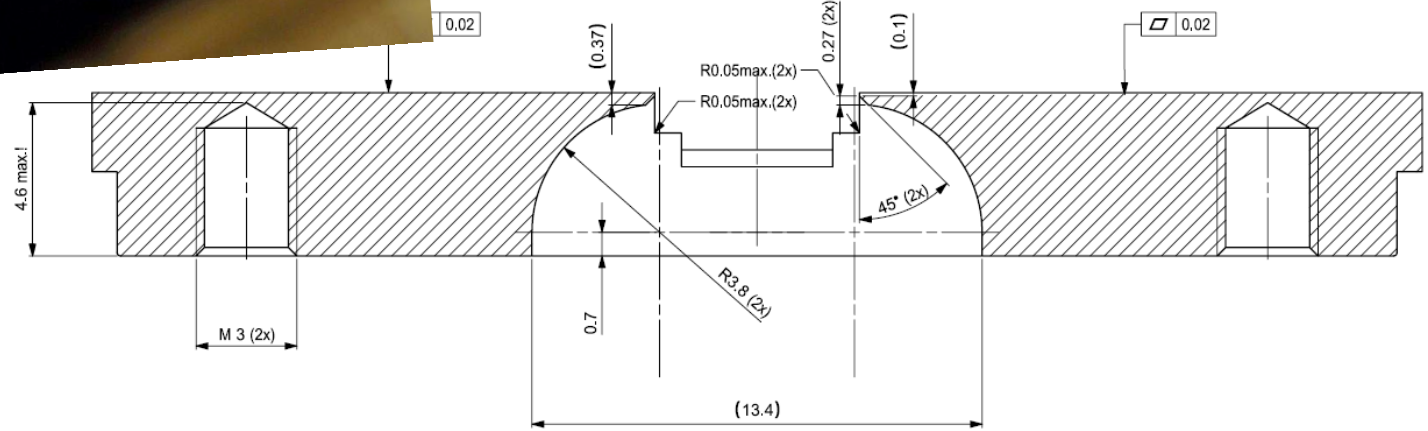


Bending wirebond PCB

- The wirebond PCB is bend downwards with 100 µm sagitta
  - Only supported at both ends
  - Pushed down in the middle by the flex
- Next PCB design we have to increase the distance between PCB surface and flex
  - Now: 1.2 – 1.3 mm







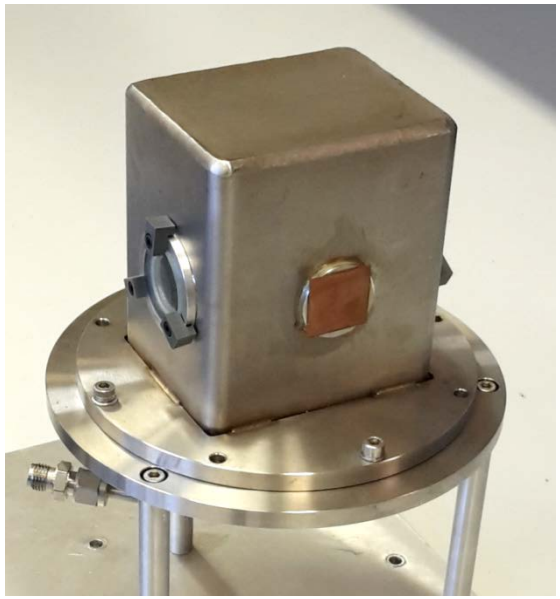
Finishing electrical QUAD 2

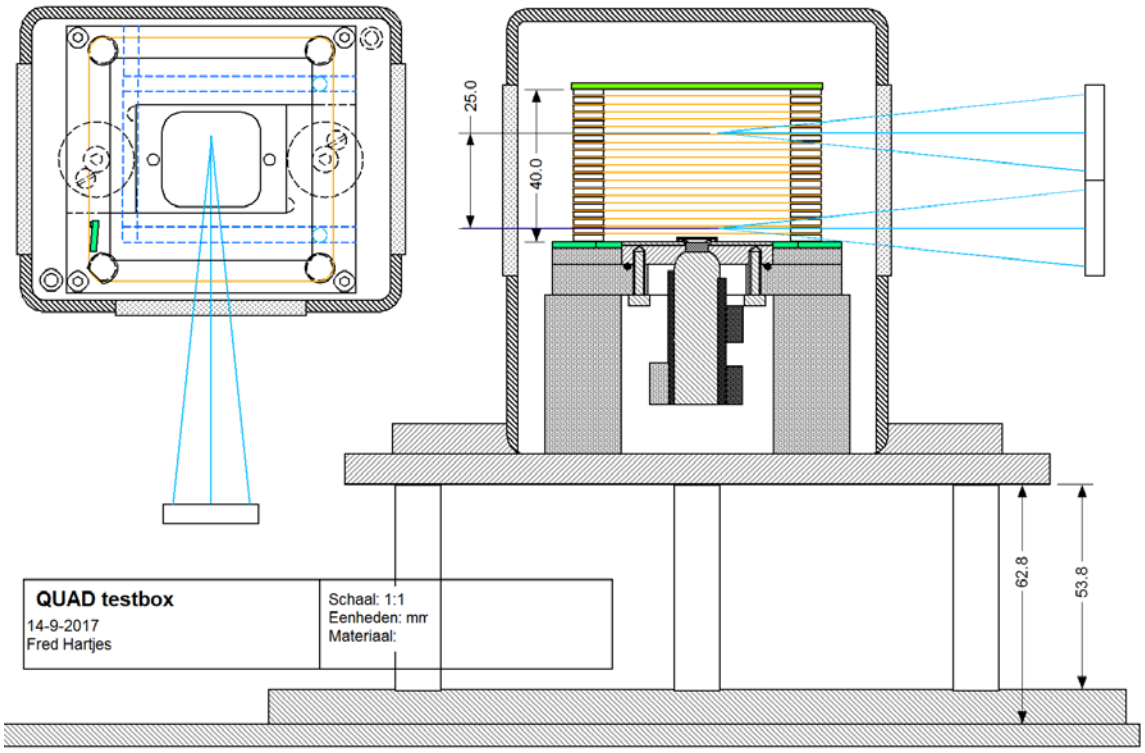
- According to Jochen's mail we will get this week 18 chips:
  - 9 D
  - 3 C
  - 2 B
  - 4 A
- Since we still have components to populate 2 electrical QUADs my suggestion is to use for QUAD 2 and QUAD 3:
  - 2 A
  - 1 B
  - 1 C
- This leaves us for spare in case of failure
  - 9 D
  - 1 C
- In principle I could finish QUAD 2 within 1 week
  - But as a safety we might wait until Bas can communicate with QUAD 1
  - We do not need QUAD 2 earlier than after finishing the testbox i.e around October 6

Testbox for single QUAD

- Intended for UV laser measurements
- Components in production
  - Expected this week
  - Assembly ~ 1 week

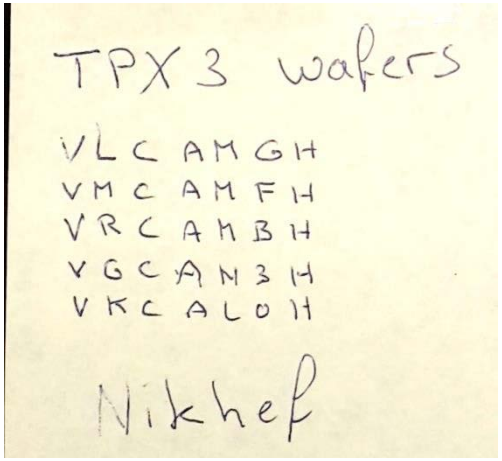
- On laser setup two new 50 mm actuators installed
  - 50 x 50 mm in XY plane
  - Covering the full QUAD surface
  - 25 mm range in Z
  - LabVIEW control to be updated (Kevin)





TPX3 wafers at Nikhef

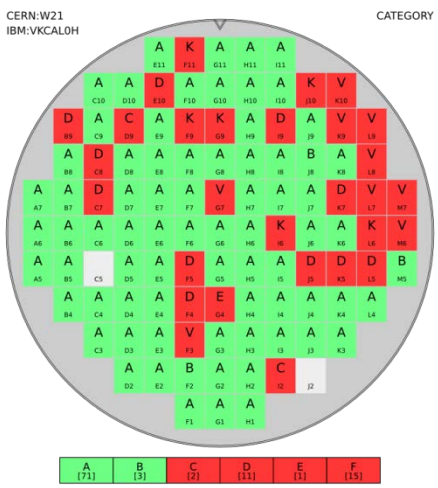
- 5/6 wafers sent to Nikhef on July 31, 2015 (Jan Visser)
- High yield wafers
  - Average 78 out of 105 good chips (A or B) per wafer (74%)
- Costs: 2620 CHF/wafer
- We have had already one low yield wafer (W16?)
- Waiting for contact with persons in charge before sending two to Yevgen

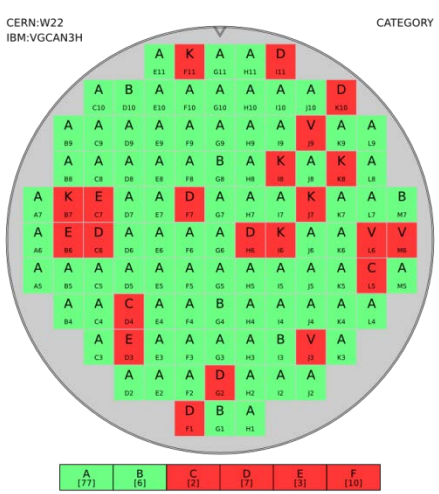


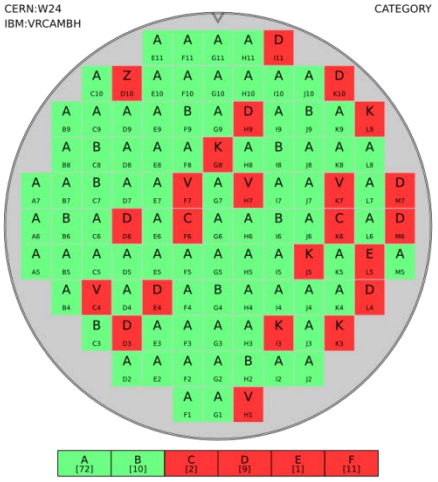
IBM number	Date Code	CERN number	Tested	When	A	B	C	D	E	F
VTCAQQH	1528	W020	Yes	23-7-2025	75	6	5	4	2	13
VKCAL0H	1528	W021	Yes	23-7-2025	71	3	2	11	1	15
VGCAN3H	1528	W022	Yes	24-7-2015	77	6	2	7	3	10
VRCAMBH	1528	W024	Yes	27-7-2016	72	10	2	9	1	11
VMCAMFH	1528	W025	Yes	28-7-2015	66	7	8	6	1	17
VLCAMGH	1528	W026	Yes	28-7-2015	72	4	8	4	2	15

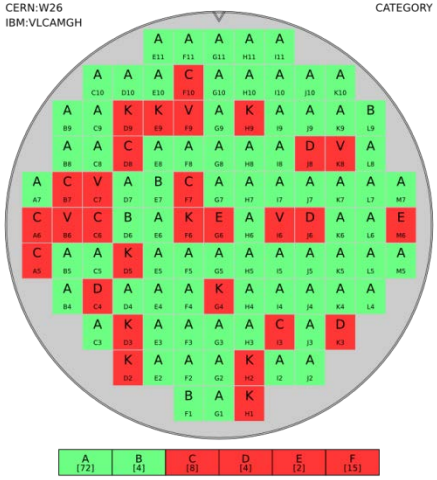
Wafer maps

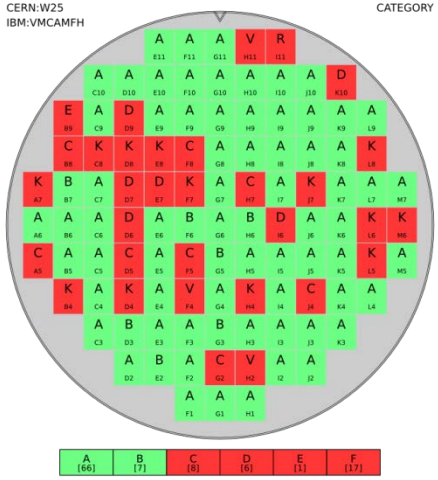
- Made by Jerome Alozy (CERN)





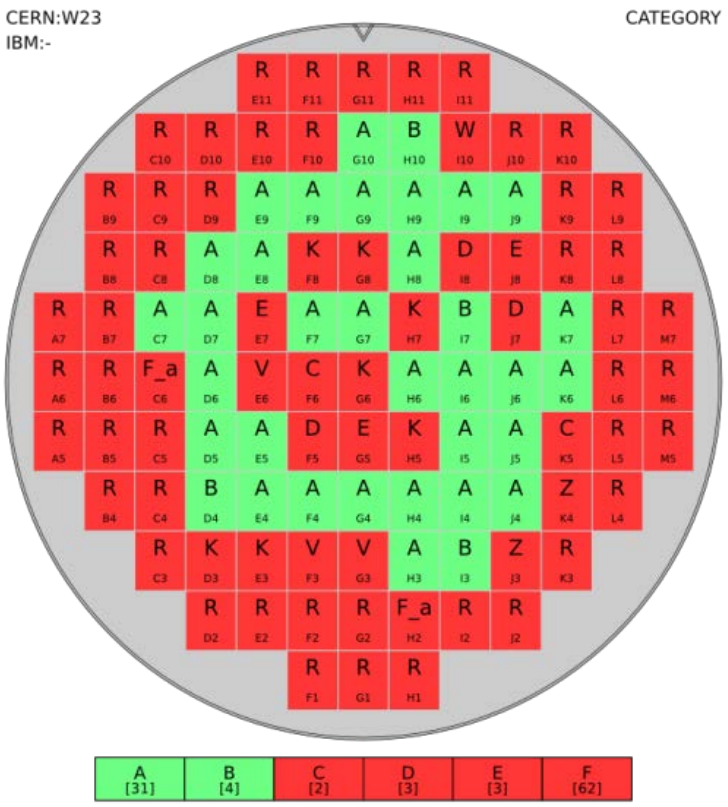






Another low yield wafer?

- Chips are mainly class A or F
- 35 good chips (class A (B)
  - 45% of high yield wafer
- Only 8 class C, E or E
- 62 class F chips (59%)



Assembly frame

- 25 x 25 mm holes
- Cooling by pipes in the frame
  - Excellent thermal contact between chips and cooling channels