

# Review Comment Bullet Points

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## 1 Bullet Points

- **The Data Loading Bottleneck ( $O(N)$  Load Complexity):** Reviewer 2 explicitly requests a discussion on the  $O(N)$  load complexity required to input classical data into the quantum state, referencing Phys. Rev. D 101, 094015. We must address whether data loading negates  $O(N \log N)$  complexity and specify the runtime of the complete process.
- **Classical Timelines and Quantum Crossover ( $N$ ):** Both reviewers want quantitative details on classical algorithms. Specifically, at what value of  $N$  (number of tracks/matrix size) does the asymptotic quantum advantage actually surpass classical state-of-the-art runtimes? How does this value of  $N$  map to the actual expected HL-LHC timeline and luminosities?
- **Fault-Tolerant vs. NISQ Era Scaling:** Reviewer 3 asks for a short discussion in the Results section regarding fault-tolerant scenarios. Would conclusions about hardware connectivity (trapped-ion vs. superconducting) hold up when considering the scaling of fault-tolerant logical qubits and their noise floors?
- **Generality of the Method:** Reviewer 2 and 3 both ask how generalizable the 1-Bit QPE/spectral filtering method is. Does this conceptual advance apply to other classes of physics/optimization problems beyond this specific toy model? Also, does the Hamiltonian sparsity assumption hold up under full HL-LHC conditions?
- **Expanding Limitations in Realistic Detectors:** While we already addressed missing hits, Reviewer 2 wants a more prominent discussion (in the Intro and Discussion) regarding other messy realities of physical detectors: multiple scattering, non-Gaussian uncertainties, and detector inefficiencies.
- **Physics Context for Non-Experts:** Reviewer 3 wants an explanation on why extracting Primary Vertices ( $z$ -vertices) is useful information on its own. This is obvious to an LHC experimentalist but not to the general QC4HEP audience.
- **Hardware Execution (If possible):** Reviewer 2 strongly suggests running a small, proof-of-principle implementation on actual quantum hardware rather than just emulators, given that our circuit depths allow for it.