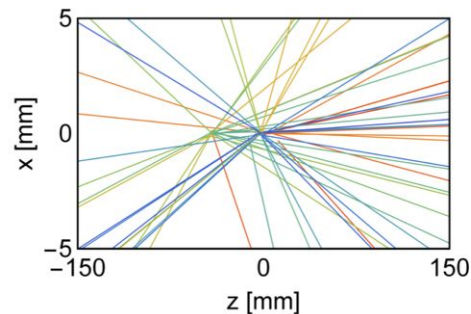
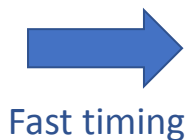
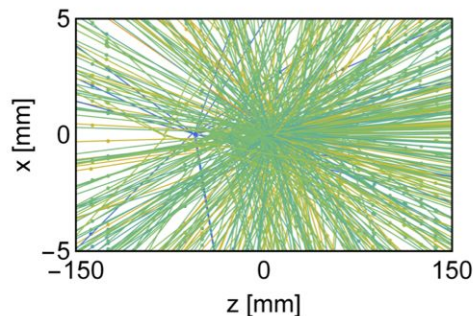
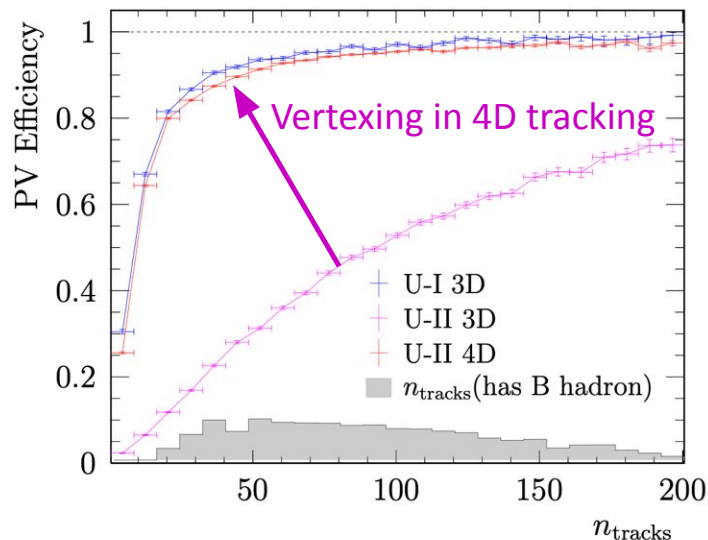


FastTrack Kickoff Meeting

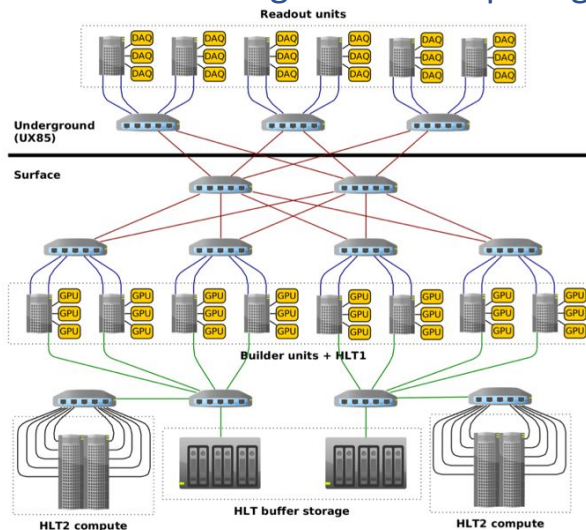
LHCb



Cost LHCb U2:



Sustainable heterogeneous computing:



Detector

VELO
UT
Magnet Stations
MT-SciFi
MT-CMOS
RICH
TORCH
ECAL
Muon
RTA
Online
Infrastructure
Total

Request to NWO (kCHF)

VELO

- Sensors** ←
- ASICS** ←
- hybridisation
- Optical links and feedthroughs
- Opto and Power boards
- Data Acquisition and Controls** ←
- Power Supplies
- RF foil** ←
- cooling plant
- Vacuum and Motion
- Cooling
- Modules** ←
- Detector Layout and Construction** ←
- total (k€)

LHCb FTDR	Nikhef Contribution	Requested Budget
	50%	
	50%	
	0	
	0	
	0	
	50%	
	0	
	100%	
	0	
	0	
	0	
	50%	
	33%	
	34.1%	

- [redacted] As contribution to VELO detector
- [redacted] M in contributions to the LHCb common Fund
 - Online and DAQ infrastructure
 - Explore distributed HLT2 option

**Total MOU of [redacted] M
(Consistent with M&O share)**

- R&D
- prototyping
- Computing
- infrastructure

Total Nikhef of [redacted]

Envelope [redacted] M

Projects under the LHCb VELO Upgrade 2

Module and Cooling R&D → Velo Module Development

Development of Module substrates, cooling, electronics, readout and testing procedures

Detector Design → Velo Detector Mechanics

Design of the detector layout, vacuum interfaces, detector assembly.

Sensors & ASIC R&D → VeloPix2 and 3D sensors

Picopix ASIC project and Sensor R&D will merge into Velopix2 and 3D sensors.

In terms of workforce this means the ASIC team and support for detector testing (boards, probe stations wire bonding etc)

Data acquisition → Velo DAQ and Controls

Setup FELIX approach to use in LHCb VELO; Setup DAQ system for high speed tests of picopix/velopix2 ASIC.

RF Shield R&D → RF Shield Production

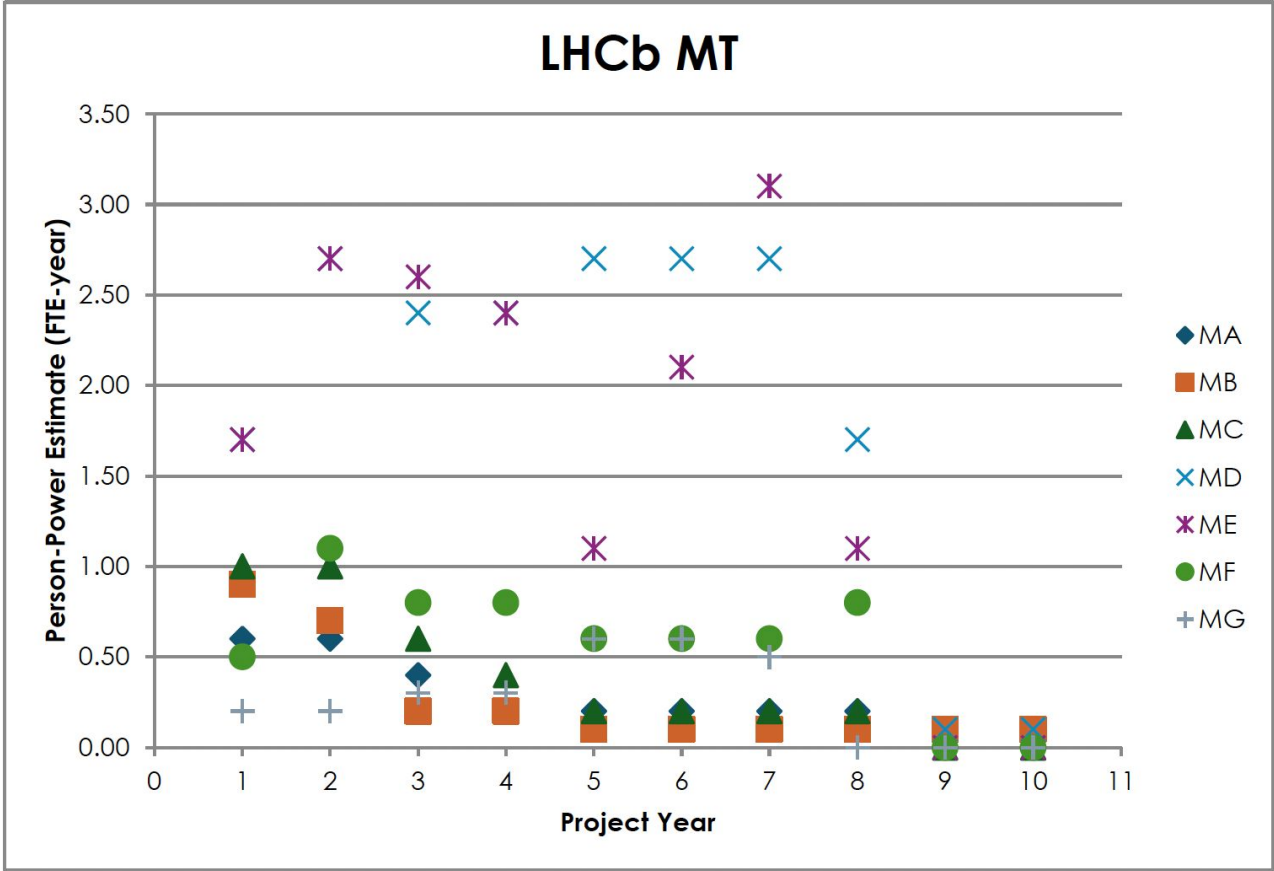
Design and manufacture the RF boxes

Workforce Estimates

Description of Activity	Nikhef Project	Deliverable Type	FASTTRACK WP	Q2/2026-Q1/2027	Q2/2027-Q1/2028	Q2/2028-Q1/2029
Sensors+ASICs	VELO Sensors & ASICs	MoU	WP1.1 3D Hybrids	0.1MD 0.1ME 0.1MG 0.2EA 1EC 1ED 0.3EE	0.1MD 0.1ME 0.1MG 0.2EA 1EC 1ED 0.3EE 0.3CB 0.3CD	0.1MD 0.1ME 0.1MG 0.2EA 1EC 1ED 0.3EE 0.3CB 0.3CD
Controls and DAQ	VELO DAQ & Controls	MoU	WP3.1 High-Speed Transmission +WP3.2 Common DAQ	0.3EA 0.7EB 0.3EE 0.4CA 0.3CB	0.3EA 0.7EB 0.3EE 0.4CA 0.3CB	0.3EA 0.7EB 0.3EE 0.4CA 0.3CB
RF Shield	VELO RF Shield	MoU	WP4.3 Mechanics & Infrastructure	0.2MA 0.2MB 0.4MC 1MD 0.2ME	0.2MA 0.2MB 0.4MC 1MD 0.2ME 0.5MF	0.1MD 0.1ME
Module Production and Cooling	VELO Module Development	MoU	WP4.1 Module Construction +WP4.2 Cooling	0.2MA 0.7MB 0.4MC 0.4MD 0.8ME 0.3MF 0.1MG 0.4EA 0.2EB 0.2EE 0.3CA 0.3CB 0.1CD	0.5MB 0.2MC 1.2MD 1.2ME 0.2MF 0.1MG 0.6EA 0.2EB 0.2EE 0.6CA 0.6CB 0.1CD	0.2MB 0.2MC 1.2MD 1.2ME 0.4MF 0.2MG 0.4EA 0.4EB 0.8EE 0.3CA 0.3CB 0.1CD
Detector Mechanics	VELO Detector Mechanics	MoU	WP4.3 Mechanics & Infrastructure	0.2MA 0.2MC 0.2MD 0.6ME 0.2MF 0.2EE 0.2CB	0.4MA 0.4MC 0.4MD 1.2ME 0.4MF 0.2EE 0.4CB	0.4MA 0.4MC 1MD 1.2ME 0.4MF 0.8EE 0.8CB
Common Funds	RTA	MoU-CF	WP5.1 Accelerators			

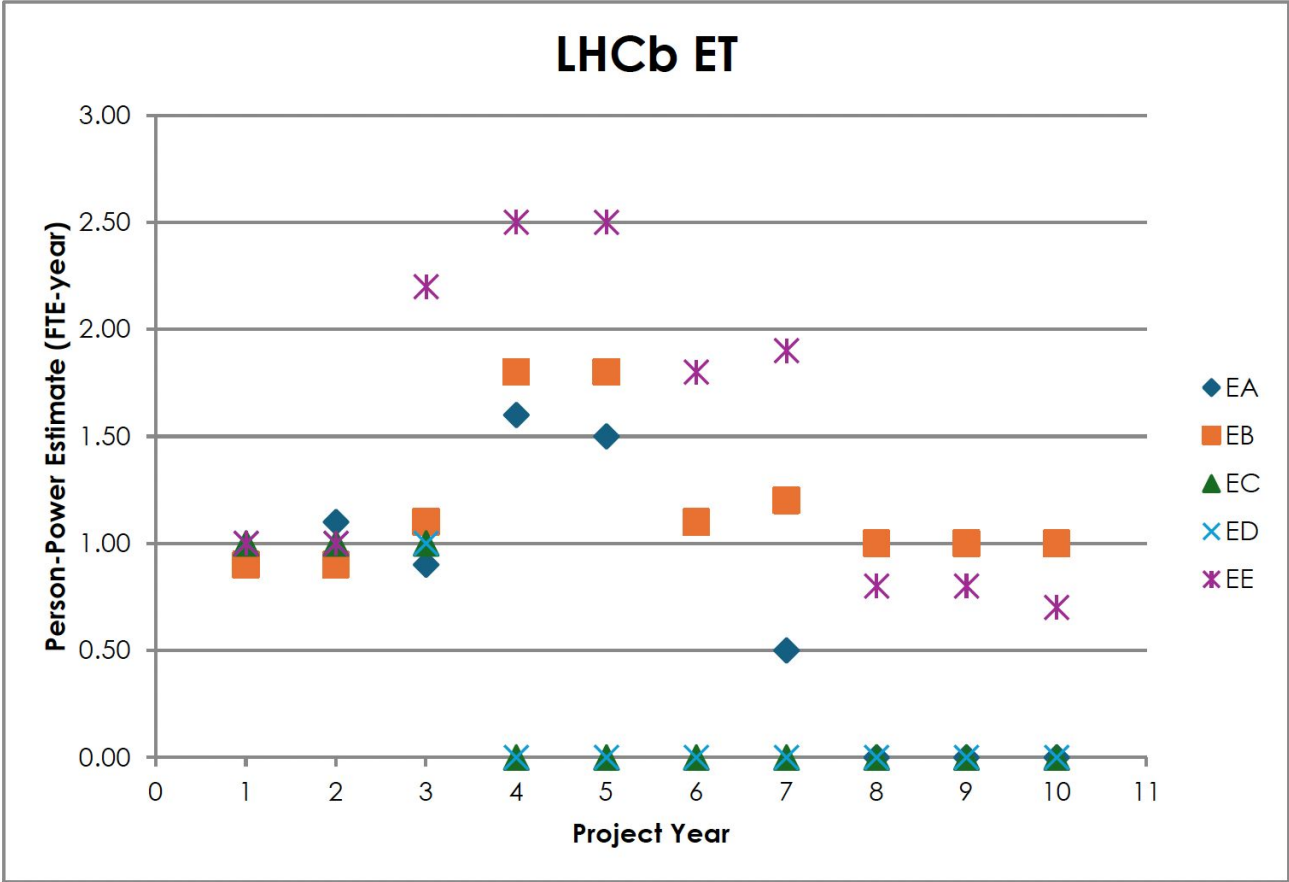
Q2/2029-Q1/2030	Q2/2030-Q1/2031	Q2/2031-Q1/2032	Q2/2032-Q1/2033	Q2/2033-Q1/2034	Q2/2034-Q1/2035	Q2/2035-Q1/2036
0.1MD 0.1ME 0.1MG 0.9EA 0.7EB 1.3EE 0.3CB 0.3CD	0.1MG 1EA 0.7EB 1.3EE 0.5CB 0.5CD	0.1MG 0.6EA 0.6EE 0.5CB 0.5CD	0.3EA 0.3EE 0.3CB 0.3CD	0.3CB 0.3CD	#N/A	#N/A
0.3EA 0.7EB 0.3EE 0.4CA 0.3CB	0.3EA 0.7EB 0.3EE 0.4CA 0.3CB	0.3EA 0.7EB 0.3EE 0.4CA 0.3CB	1EB 0.7EE 0.4CA 0.3CB	1EB 0.7EE 0.5CA 0.5CB	1EB 0.7EE 0.5CA 0.5CB	1EB 0.7EE 0.2CA 0.5CB
0.1MD 0.1ME	0.1MD 0.1ME 0.2MF	0.1MD 0.1ME 0.2MF	0.1MD 0.1ME 0.2MF	0.1MD 0.1ME 0.4MF	#N/A	#N/A
0.2MB 0.2MC 1.2MD 0.2ME 0.4MF 0.2MG 0.4EA 0.4EB 0.8EE 0.3CA 0.3CB 0.1CD	0.1MB 1.1MD 0.5MG 0.2EA 0.4EB 0.8EE 0.2CA 0.2CB 0.1CD	0.1MB 1.1MD 0.5MG 0.2EA 0.4EB 0.8EE 0.2CA 0.2CB 0.1CD	0.1MB 1.1MD 0.5MG 0.2EA 0.2EB 0.8EE 0.2CA 0.2CB 0.1CD	0.1MB 0.1MD 0.1CA 0.1CD	0.1MB 0.1MD 0.1CA 0.1CD	0.1MB 0.1MD 0.1CA 0.1CD
0.2MA 0.2MC 1MD 2ME 0.4MF 0.1EE 0.8CB	0.2MA 0.2MC 1.5MD 1ME 0.4MF 0.1EE 0.4CB	0.2MA 0.2MC 1.5MD 2ME 0.4MF 0.1EE 0.2CB	0.2MA 0.2MC 1.5MD 3ME 0.4MF 0.1EE 0.2CB 0.2CD	0.2MA 0.2MC 1.5MD 1ME 0.4MF 0.1EE 0.2CB 0.2CD	0.1EE 0.4CB 0.2CD	0.4CB 0.2CD

Workforce estimates Mechanics



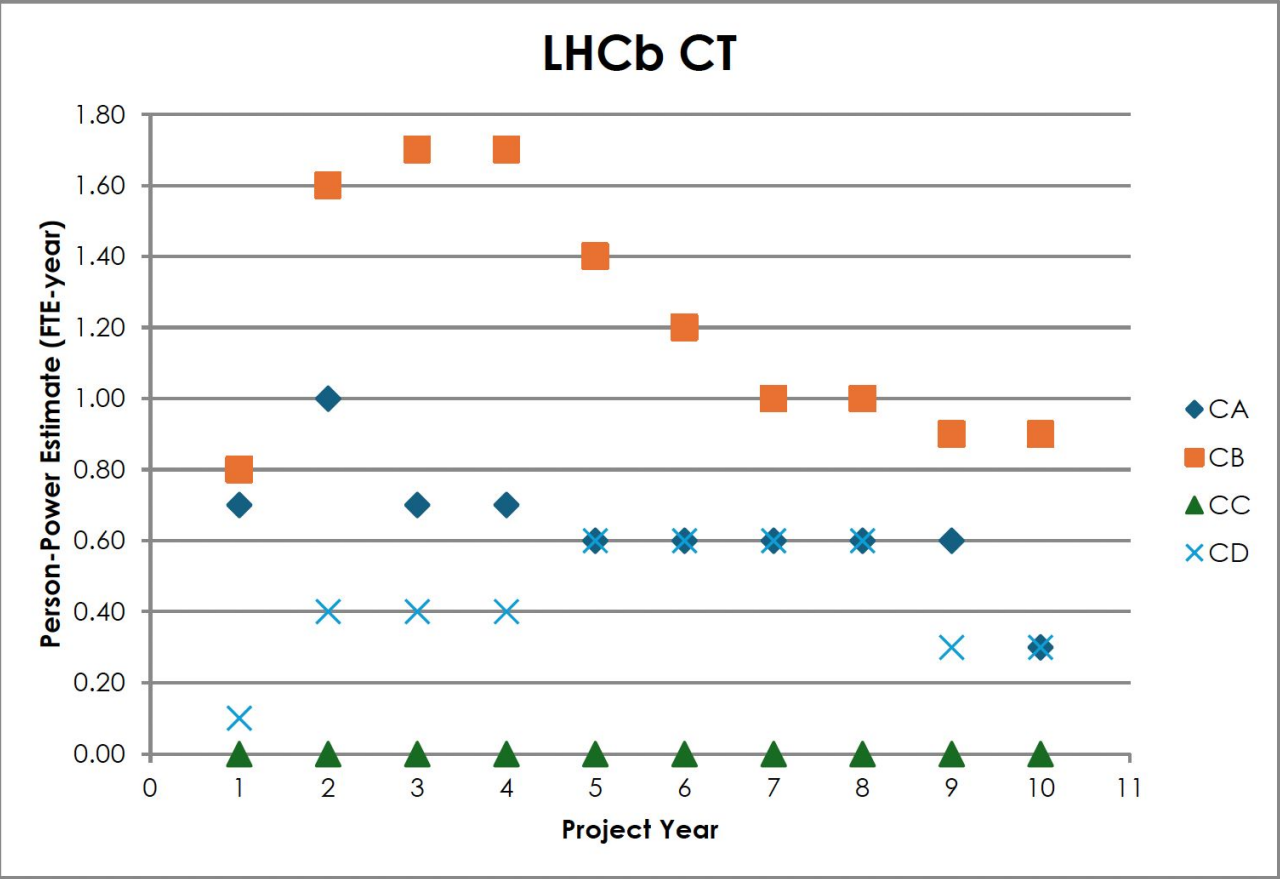
MA	Simulation studies
MB	Studies of Thermodynamics & Heat Transfer
MC	Materials Science & Engineering
MD	Manufacturing & Production
ME	Design & Drafting
MF	Control Systems & Mechatronics
MG	Wirebonding

Workforce estimates Electronics



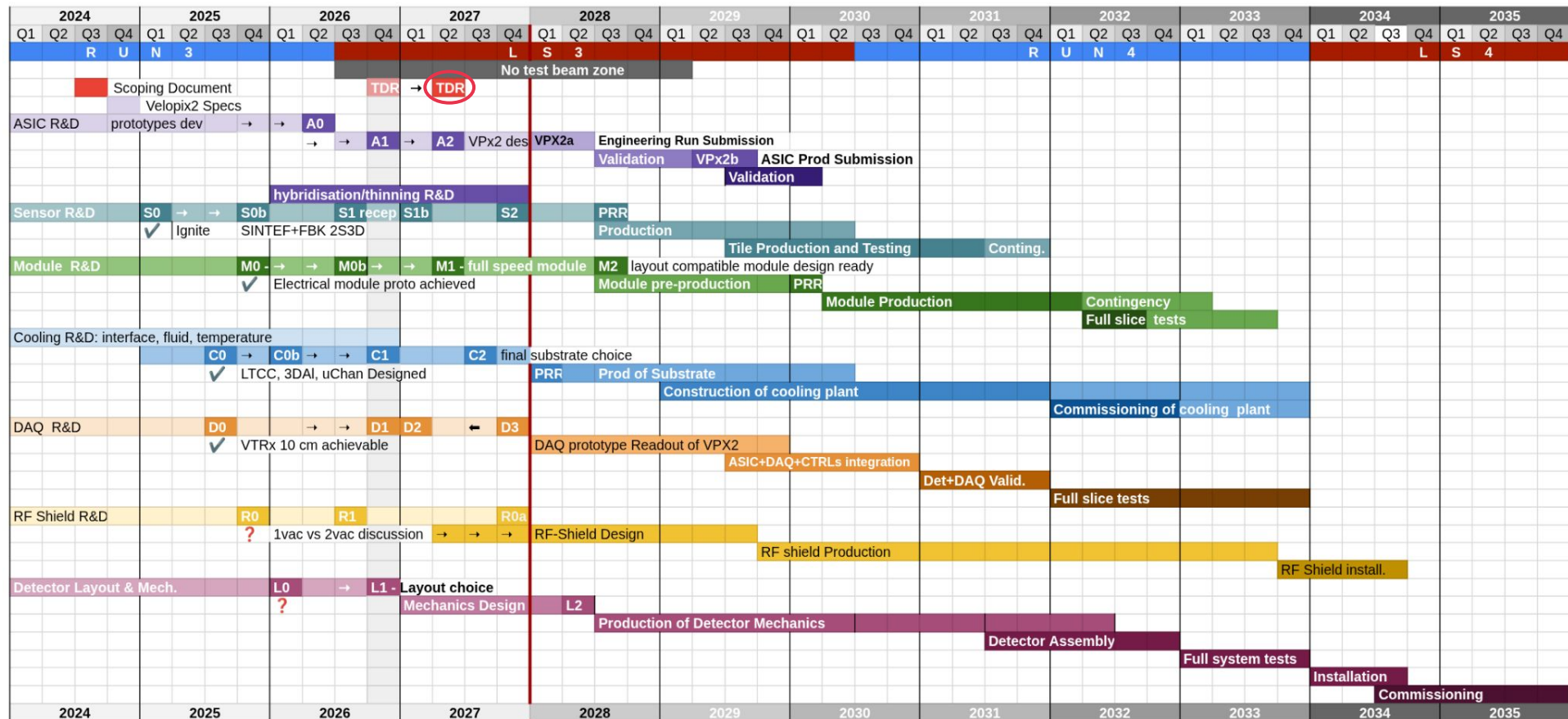
EA	Analog electronics design (frontends, RF, advanced PCB's)
EB	Digital electronics design (DAQ)
EC	Analog IC design
ED	Digital IC design
EE	Technical support (cables/mechatronics/integration etc)

Workforce estimates Computing



CA	Software engineering for embedded or data acquisition
CB	Software engineering for control systems (SCADA)
CC	Software engineering for analysis frameworks /simulations
CD	System administration and network administration support

Global Timeline of VELO Upgrade 2 (all work packages)



Global VELO Milestones

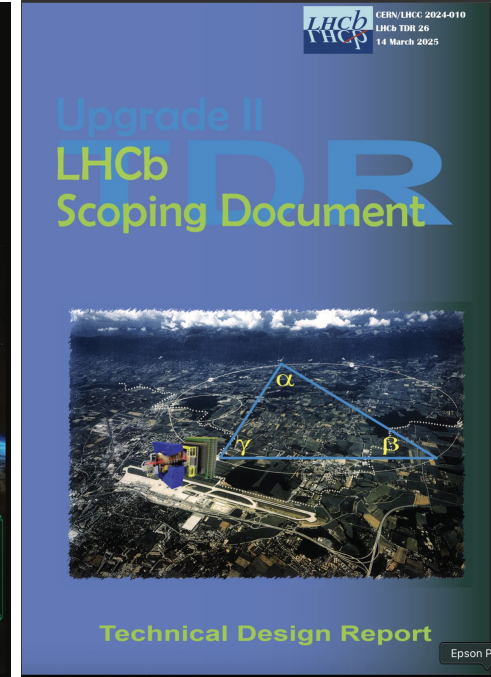
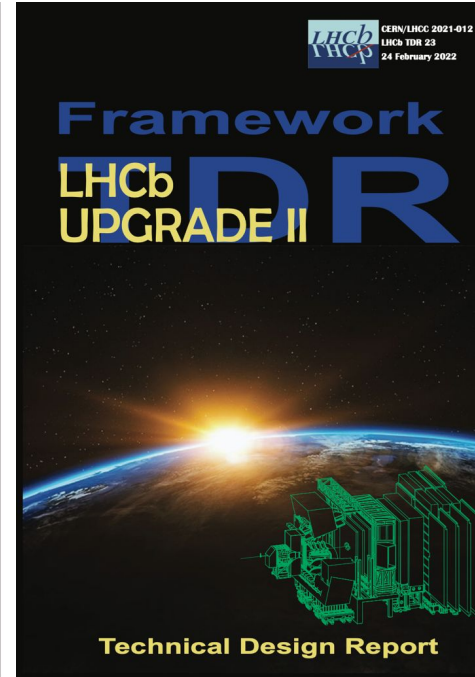
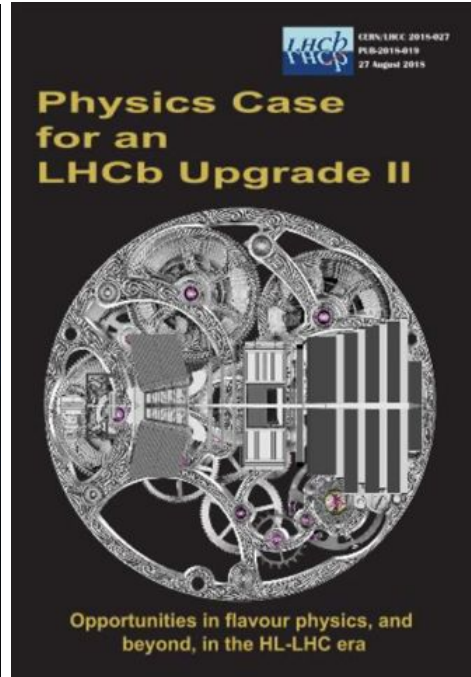
- Q2/26 **A0** PicoPix/Ignore Submission
- Q4/26 **A1** ASICs Reception and minimal testing testing phase
- Q2/27 **A2** ASIC strategy Decision

- Q1/25 **S0** FBK Sensor prototype submission
- Q4/25 **S0b** SINTEF Sensor prototype submission
- Q3/26 **S1** Sensor prototype reception
- Q1/27 **S1b** hybridization -- bump bond to ASIC prototypes
- Q4/27 **S2** Sensor prototype review -- Timing, Spatial resolution, non uniform irradiation

- Q4/25 **M0** Electrical proof of principle using timepix4
- Q3/26 **M0b** Module proof of principle using timepix4 - cooling proof of principle
- Q2/27 **M1** Single Picopix based module
- Q3/28 **M2** Tile-based, double sided Velo layout compatible module

- Q1/25 **C0** Design of cooling substrates
- Q1/26 **C0b** Evaluation and comparison of substrates
- Q2/26 **C1** choice of cooling technology - cryo+passive vs active+CO2
- Q4/27 **C2** choice of cooling substrate
- Q2/25 **D0** Decide VTRx max distance from ASIC. -- Input from VTRx indicates 10-15 cm
- Q4/26 **D1** Full speed prototype backend ready
- Q1/27 **D2** Electronics module with integrated PIC - PIC validation
- Q4/27 **D3** Decide which readout board technologies including PIC vs VTRx.
- Q1/26 **L0** Vacuum barrier technology / geometry
- Q4/26 **L1** Decision on layout approach
- Q2/28 **L2** Detector mechanics engineering design review
- Q4/25 **R0** RF -- Vacuum barrier or not?
- Q3/26 **R1** RF shield technology status review
- Q2/28 **R0a** CF replacement decision

Documents written for Upgrade 2 so far

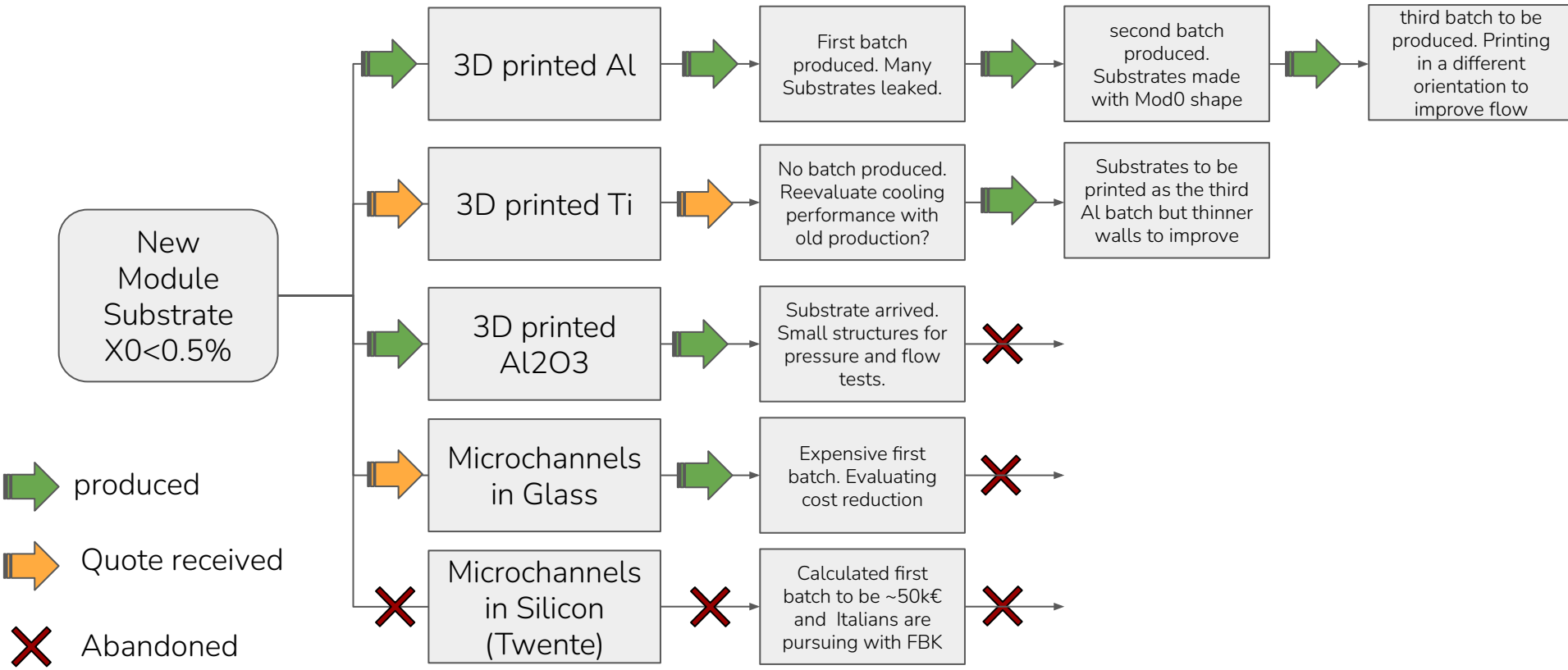


Backup

Module development -- Next 6 months

- Mechanics
 - Study of possible cooling substrate materials -- 3D printed metals
 - Cooling efficiency
 - Material budget
 - Planarity
 - Mechanical stability
 - Connectorizing
 - Study of Adhesion techniques
 - Asic-Sensor Assembly to cooling substrate
 - Brazing/Soldering adhesion to cooling substrates
 - Possible glue solutions and irradiation
 - Thermal cycling of glued/soldered parts.
- Electronics
 - Design of prototype chipboards
 - Timepix4 chipboard
 - Irradiation compatible chipboard
 - Picopix chipboard
 - Comparison between electronics materials
 - Kapton, ceramics, FR4
 - Module 0 and Module 1 are conceived as LHC-like electronics (rad hard/cern components). They require boards with lpGBT.

Module Substrate R&D Status



Detector Design -- Next 6 months

- Nikhef Layout:
 - We decided to approach the problem through a conservative angle, keeping the detector in secondary vacuum.
 - Design 2 half approach including 2 separate vacua with a boxes to separate..
 - We will review the design created for the roadmap proposal and make it more realistic.
- Global LHCb involvement:
 - Nikhef is deeply involved in the detector mechanics. Two main approaches to the detector require realistic comparisons to get feedback to simulations. Conversely the simulations will point the best solutions for physics.
 - Review the single vacuum design proposed by CERN (Detectors in the LHC vacuum)

DAQ -- Next 6 months

Module0 (TPX4) and Module1 (PPX) require lpGBT communication and because of this, a dedicated Backend. At Nikhef we decided to use FELIX.

This development demands ET and CT collaboration in testing and writing firmware/software for FELIX.

DAQ fast links under development. Picopix has 12.5 Gbps on copper and 25 Gbps through fiber. → We have been involved in the serializer design and probably would like to participate in this characterisation.

Sensors And ASICs → Next 6 months

- Final verification of PicoPix ASIC - To be submitted in Q2/26
- Test chipboards to be designed and produced -- this is independent of the DAQ system which is developed in parallel.
- Sensor designs to be submitted/produced in industry. Expected delivery on Q4/26.

RF-Box -- Next 6 months

Project On Hold, waiting for input from Oxford for technological decision.

-- project is funded under roadmap.

Simulation

Decisions on the hardware design require a lot of effort from the simulation.

At the moment, from Nikhef, there is only Tim contributing to this.

Request to NWO (kCHF)

VELO

- Sensors** ←
- ASICS** ←
- hybridisation
- Optical links and feedthroughs
- Opto and Power boards
- Data Acquisition and Controls** ←
- Power Supplies
- RF foil** ←
- cooling plant
- Vacuum and Motion
- Cooling
- Modules** ←
- Detector Layout and Construction** ←
- total (k€)

LHCb FTDR	Nikhef Contribution	Requested Budget
	50%	
	50%	
	0	
	0	
	0	
	50%	
	0	
	100%	
	0	
	0	
	0	
	50%	
	33%	
	34.1%	

- As contribution to VELO detector
- in contributions to the LHCb common Fund
 - Online and DAQ infrastructure
 - Explore distributed HLT2 option

**Total MOU of M
(Consistent with M&O share)**

- R&D
- prototyping
- Computing
- infrastructure

Total Nikhef of

Envelope