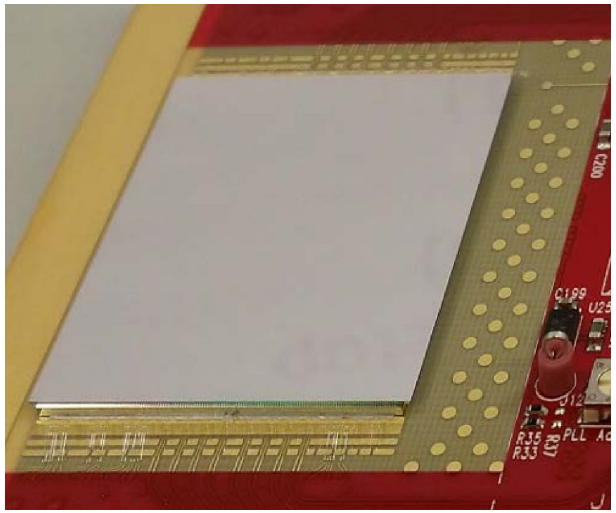
FelixSpidr Readout

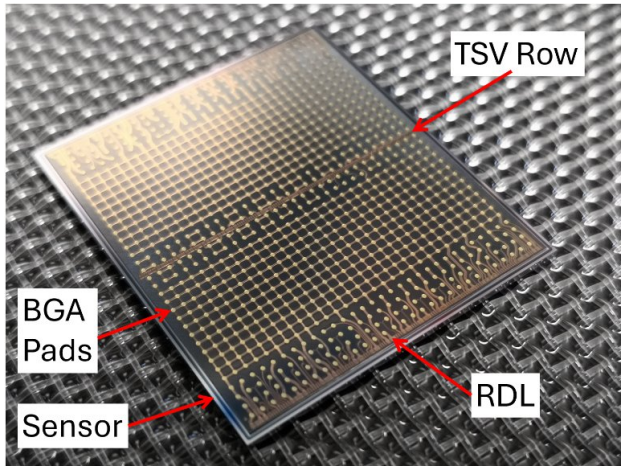
- Timepix4 specs
- Current Spidr4 system
  - Spidr4 controlboard
  - Spidr4 DAQ system
- FELIX
  - Architecture
  - LpGBT
- FelixSpidr
  - Status
  - Lab setup

Timepix4 specs

			Timepix3 (2013)	Timepix4 (2019)
Technology			130nm – 8 metal	65nm – 10 metal
Pixel Size			55 x 55 µm	55 x 55 µm
Pixel arrangement			3-side buttable 256 x 256	4-side buttable 512 x 448
Sensitive area			1.98 cm^2	6.94 cm^2
Readout Modes	Data driven (Tracking)	Mode	TOT and TOA	
		Event Packet	48-bit	64-bit
		Max rate	0.43x10^6 hits/mm^2/s	**3.58x10^6 hits/mm^2/s**
		Max Pix rate	1.3 KHz/pixel	**10.8 KHz/pixel**
	Frame based (Imaging)	Mode	PC (10-bit) and iTOT (14-bit)	CRW: PC (8 or 16-bit)
		Frame	Zero-suppressed (with pixel addr)	Full Frame (without pixel addr)
		Max count rate	~0.82 x 10^9 hits/mm^2/s	~5 x 10^9 hits/mm^2/s
TOT energy resolution			< 2KeV	< **1Kev**
TOA binning resolution			1.56ns	**195ps**
TOA dynamic range			409.6 µs (14-bits @ 40MHz)	**1.6384 ms** (16-bits @ 40MHz)
Readout bandwidth			≤5.12Gb (8x SLVS@640 Mbps)	**≤163.84 Gbps (16x @10.24 Gbps)**
Target global minimum threshold			<500 e^-	<500 e^-



Timepix4 WB with Si sensor

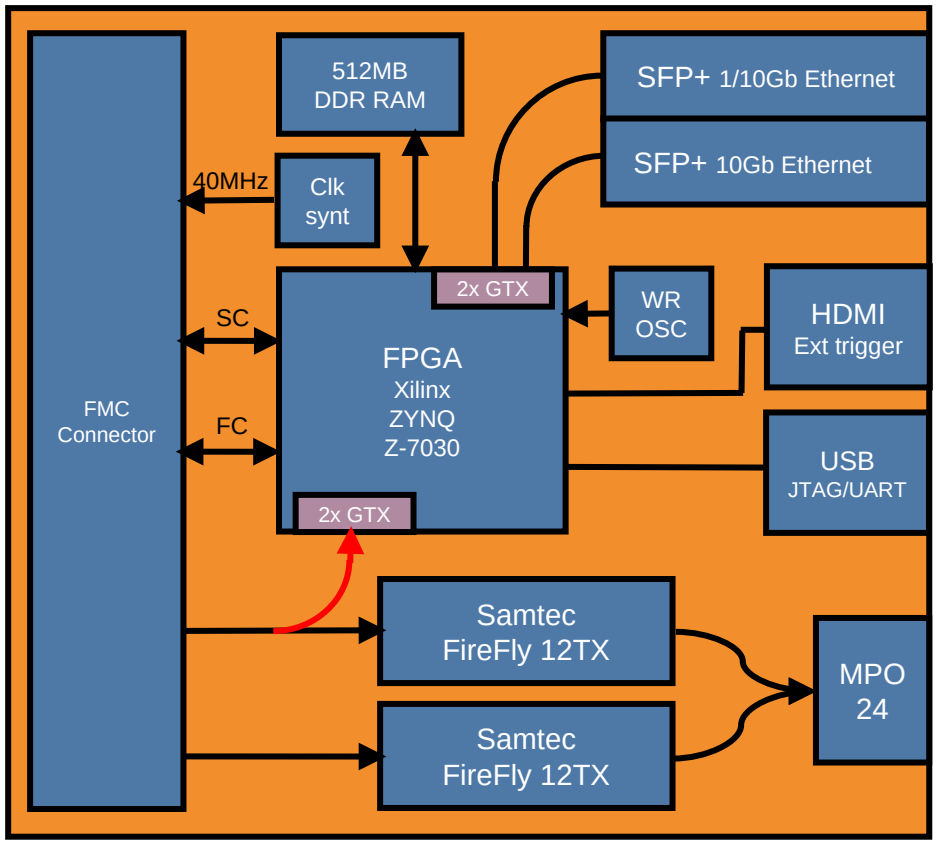


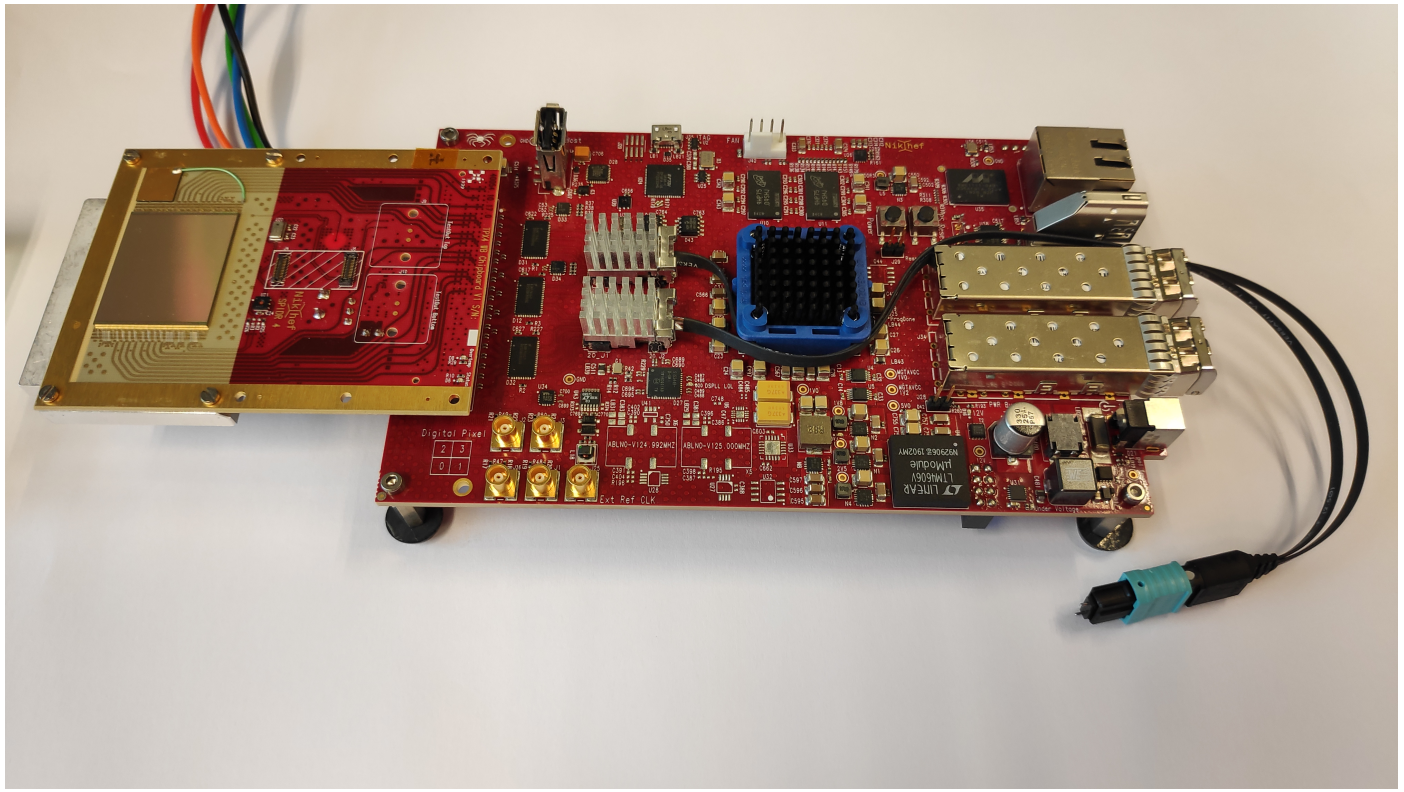
Timepix4 BGA backside

Current Spidr4 readout

- “Desktop” system to read out one Timepix4.
- 1Gb Ethernet for control using gRPC.
- 10Gb Ethernet for data acquisition (2 links from TPX4@2.56Gb/s) using UDP.
- Handles all Fast/Slow control signals for one TPX4.
- Additional “Fast DAQ” possible trough FireFly modules. (16ch@5.12Gb/s)
- Multiple Spidr systems can be synchronized.
- Many tools and scripts exist to control the TPX4.

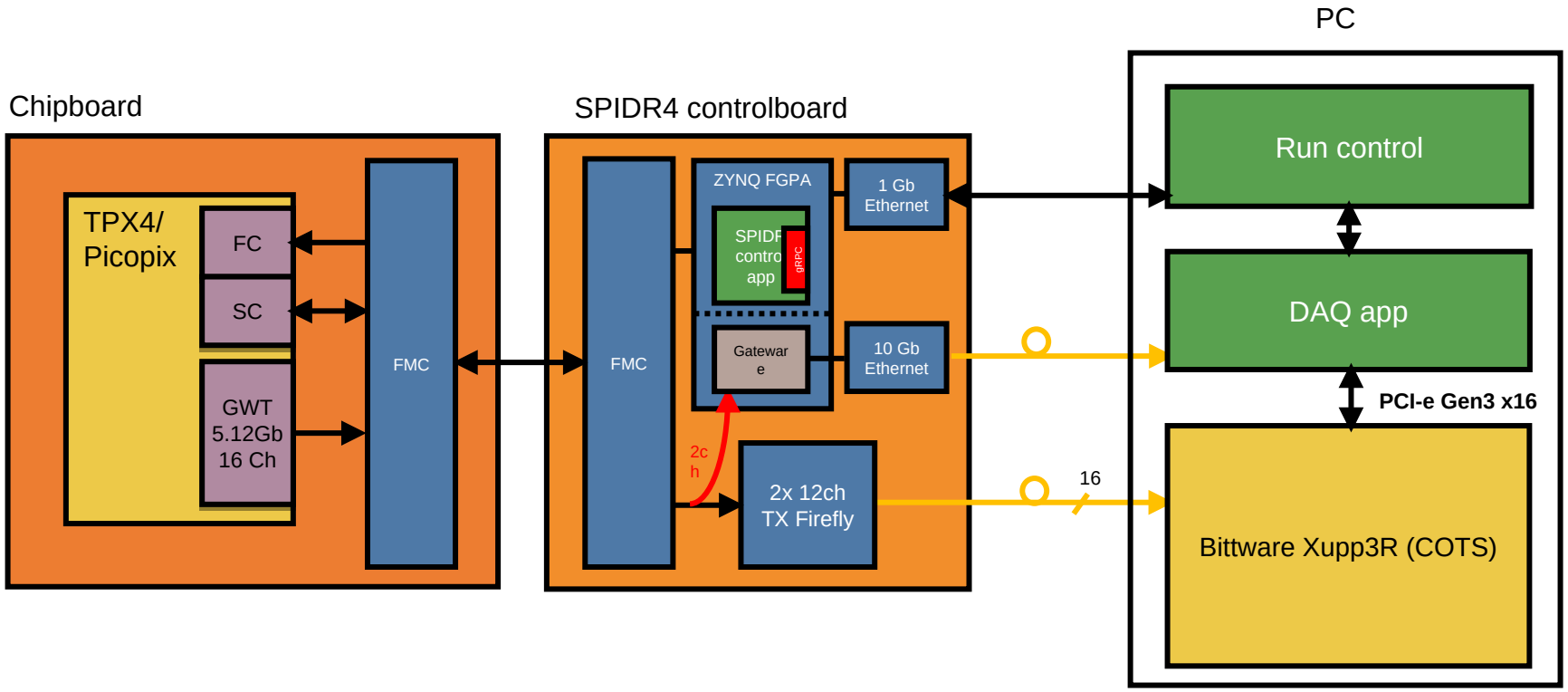
Spidr4 Controlboard





Spidr4 Controlboard and Chipboard

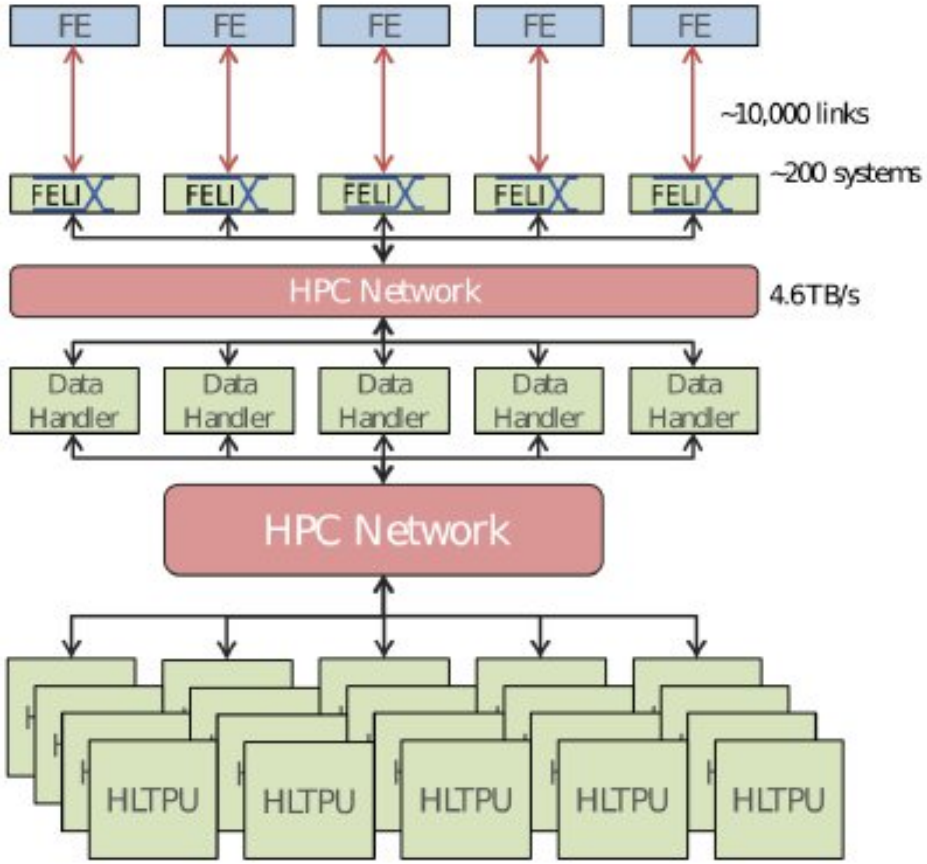
Spidr4 DAQ



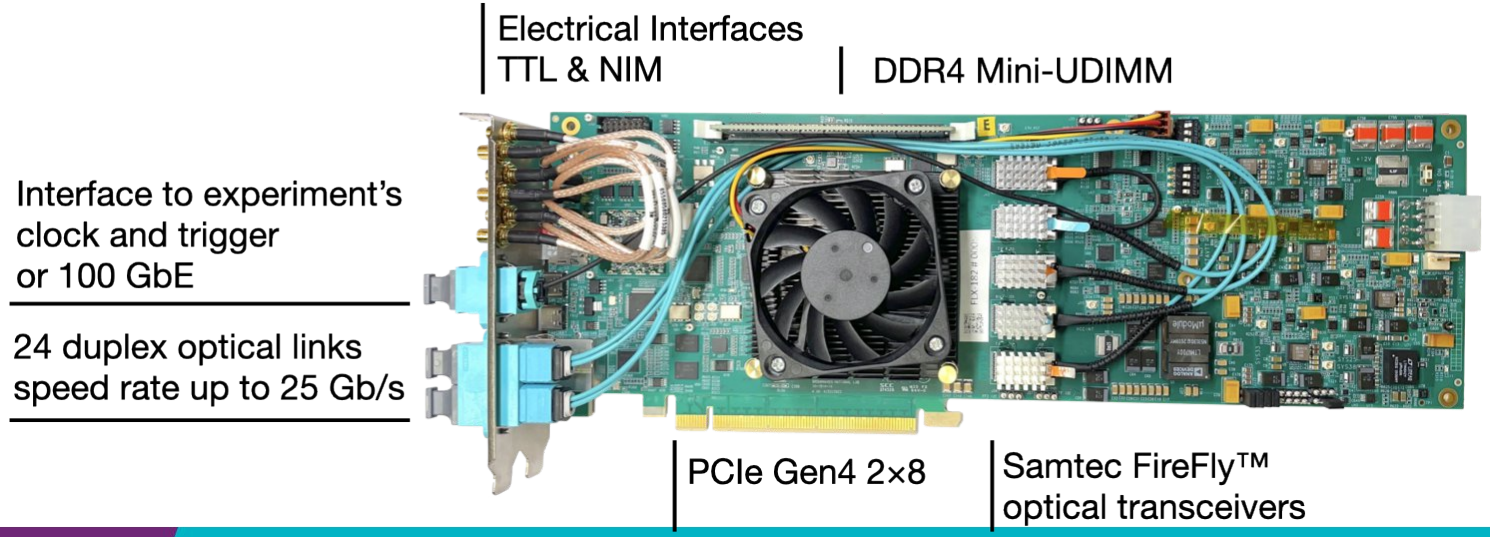
- Bittware XUP-P3R
- AMD VU9P FPGA
- COTS ~9K€
- 16lanes @5.12GB/s

The ATLAS FELIX Project

Front-End Link eXchange (FELIX)
- Implemented for all subdetector systems
- x10 trigger rate (1 MHz)
- x3 interactions per bunch crossing (200)
- x20 readout data rate (4.6 TB/s) Data Handlers
- Evolution of SW ROD with similar functionality
- Interfaces to the high level trigger farm

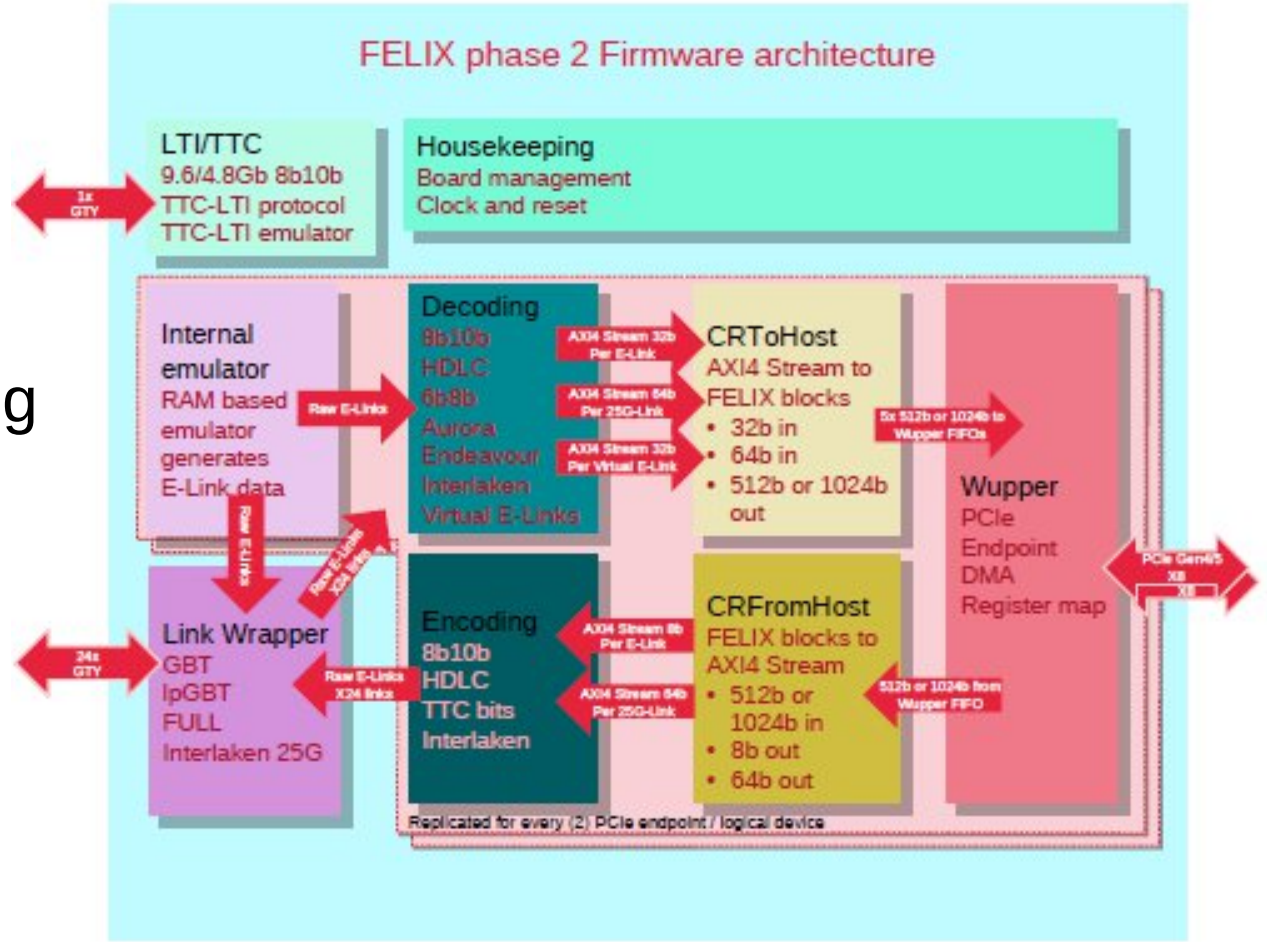


FLX-182 FELIX Card
AMD Versal Prime VM1802 system-on-chip



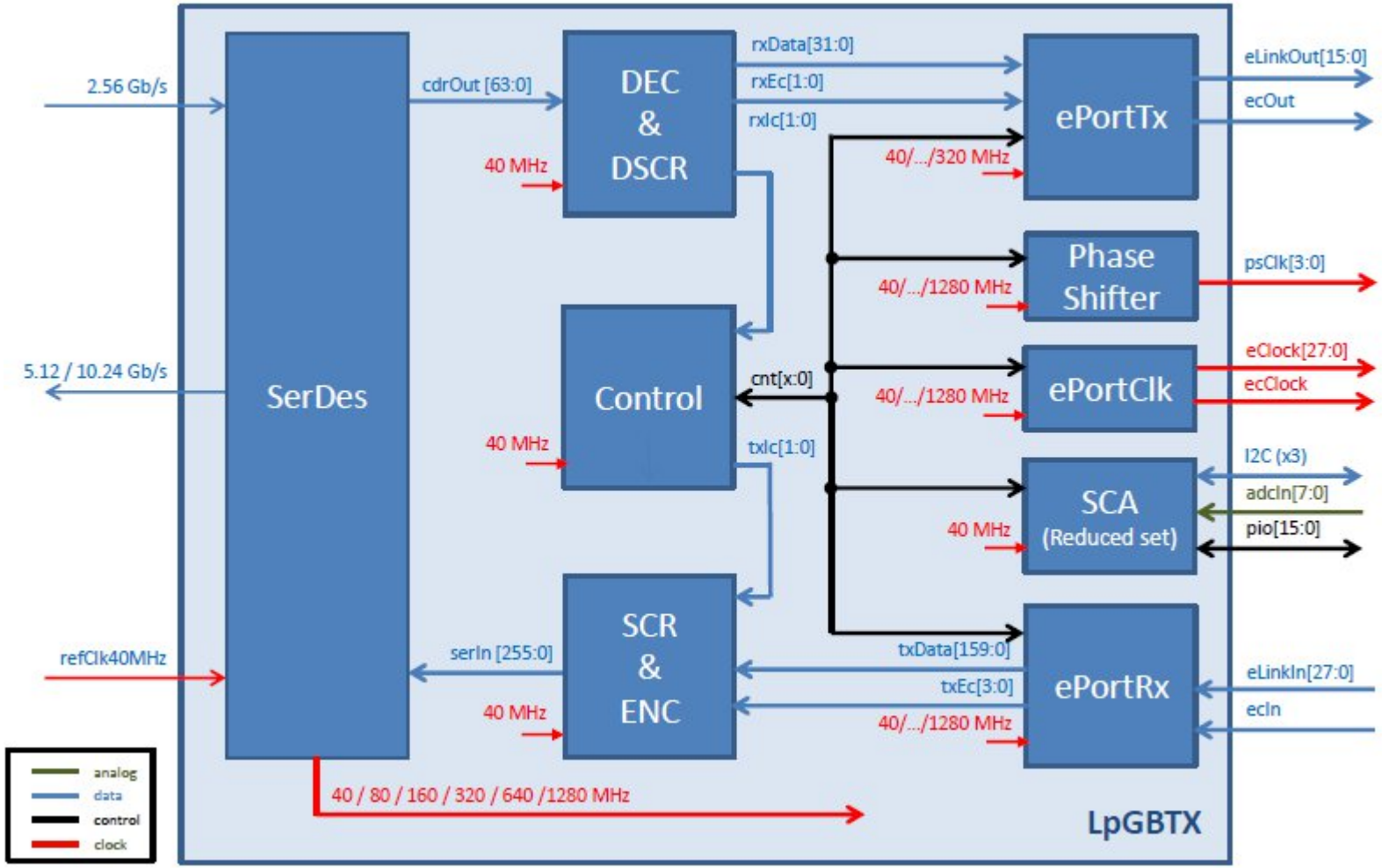
The ATLAS FELIX Project

Modular design in VHDL
- Wupper PCIe DMA core + registermap
- AXI4 Stream based design for generic components (CRToHost /CRFromHost)
- Subdetector specific decoding / encoding
- Open source
- Same source code targeting at least 6 different PCIe cards

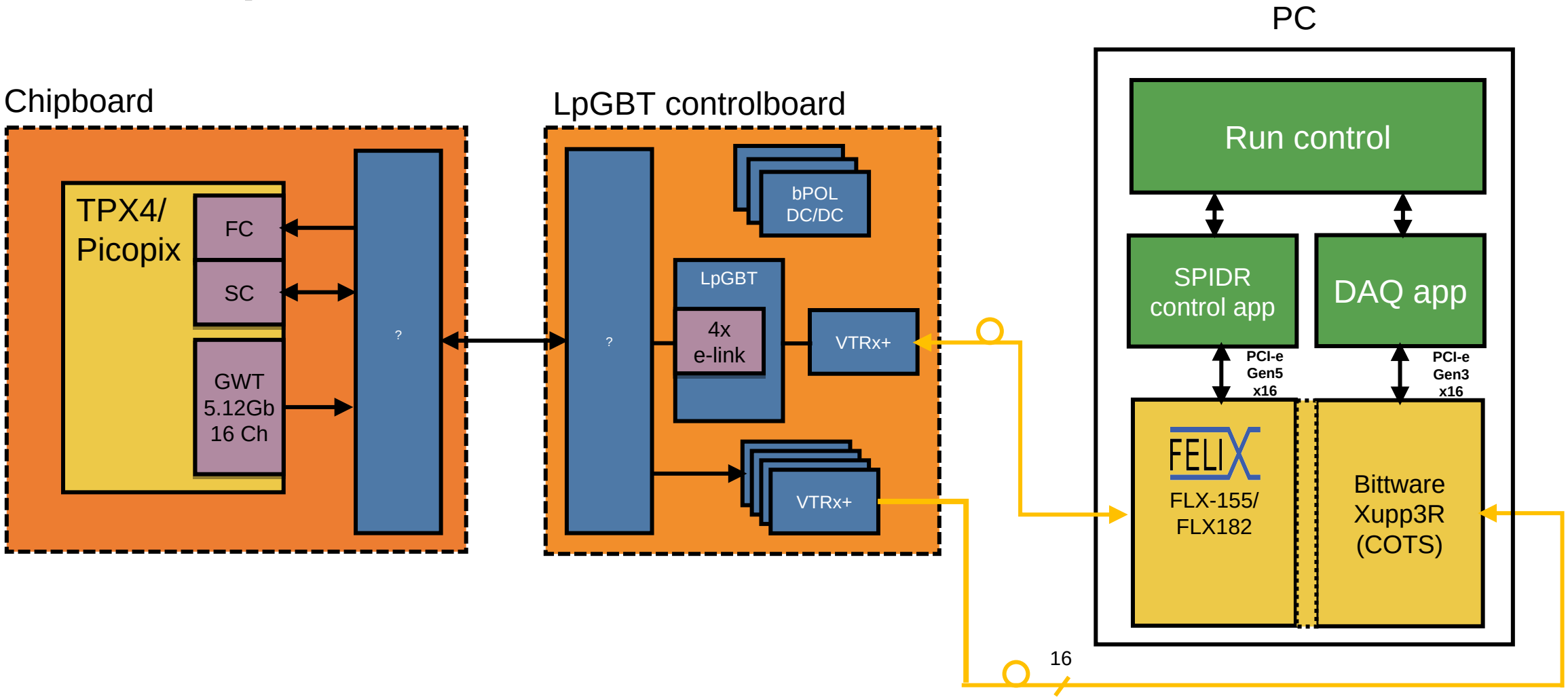


LpGBT

- Cern design
- Rad hard
- 9 x 9mm BGA Package
- Provides SC/FC signals trough 16 E-links
- 4 TPX4 per LpGBT



FelixSpidr


PC
Chipboard
LpGBT controlboard
Run control
SPIDR control app
DAQ app
PCI-e Gen5 x16
PCI-e Gen3 x16
TPX4/ Picopix
FC
SC
GWT 5.12Gb 16 Ch
?
?
bPOL DC/DC
LpGBT
4x e-link
VTRx+
VTRx+
FELIX
FLX-155/ FLX182
Bittware Xupp3R (COTS)
16

FelixSpidr status

- Felix Gateware currently under development.
- Control application is ported.
- Existing scripts and tools can still be used through gRPC.
- Investigating WinCC control through OPC UA.
- Combined SC and DAQ in one FLX.
- Multiple TPX4 capable.
- Starting design of the LpGBT controlboard.
- Future PicoPix support.
- The lab setup.

The “bricolage”