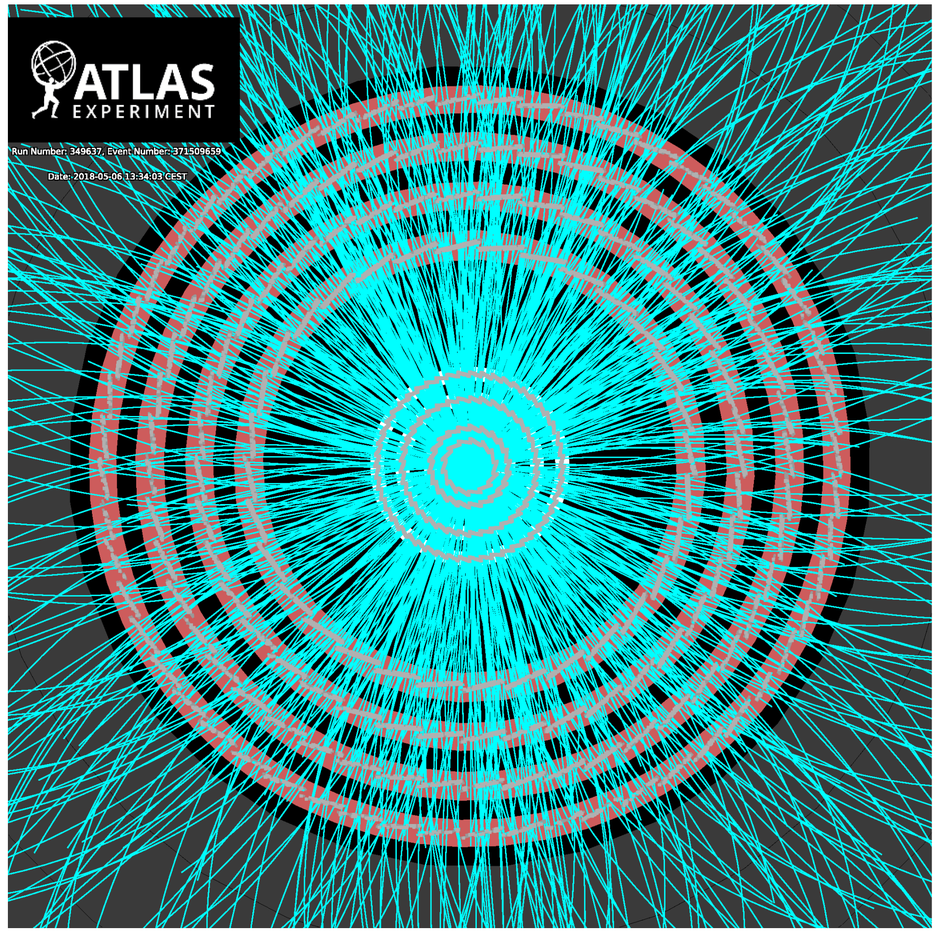
Nikhef Radboud Universiteit

ATLAS EXPERIMENT

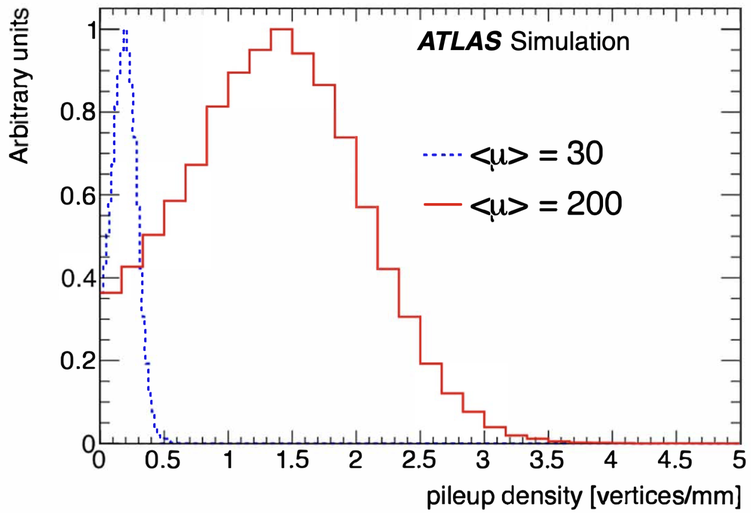


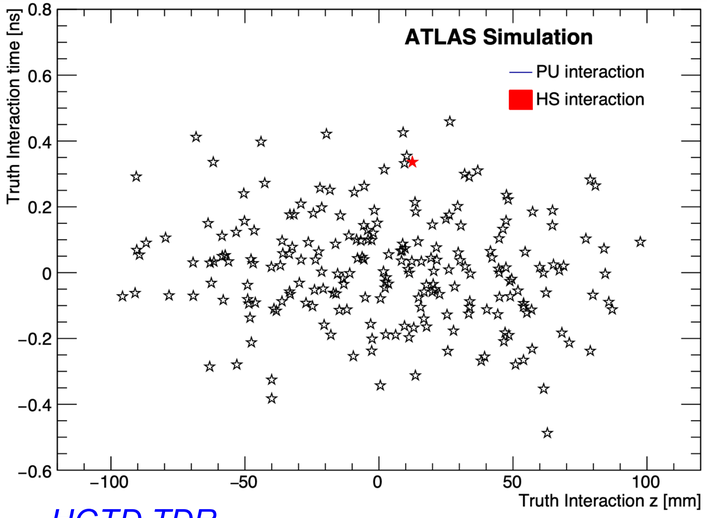
Tao Wang

Nijmegen FASTER Meeting, Sep 24th, 2025

HGTD Calibration Overview

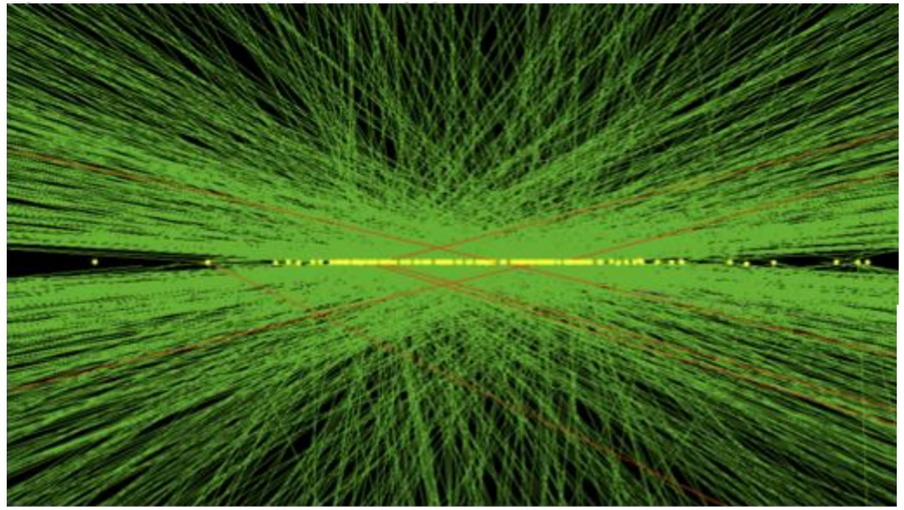
Motivation

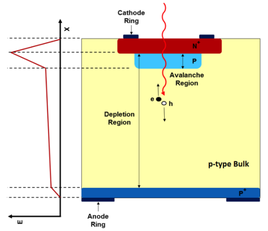


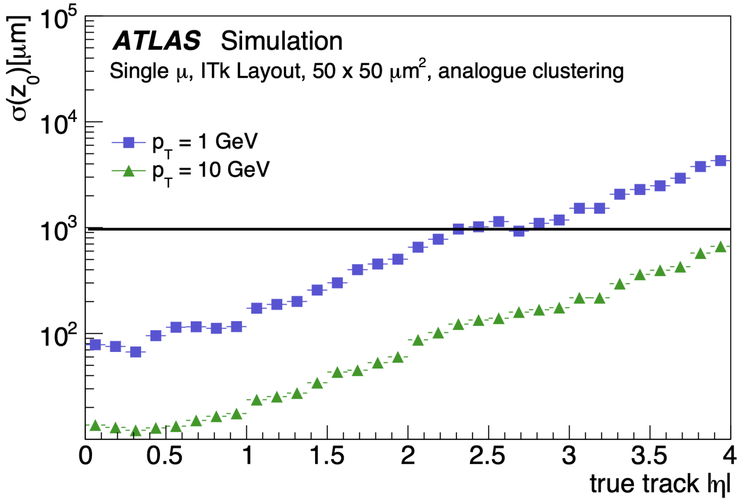


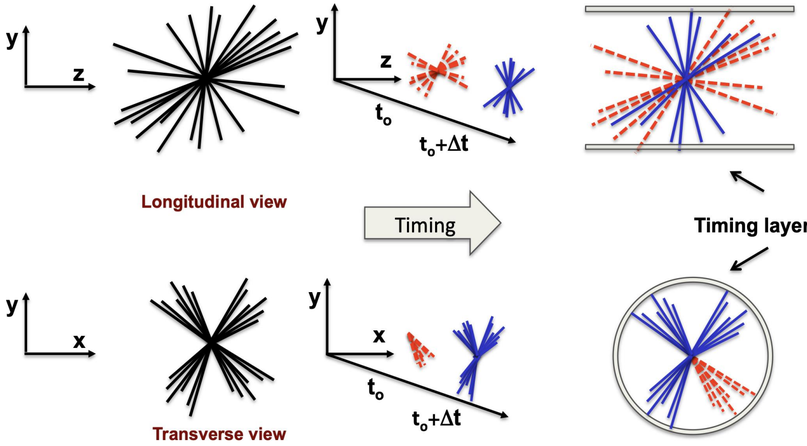
[HGTD TDR]

HL-LHC



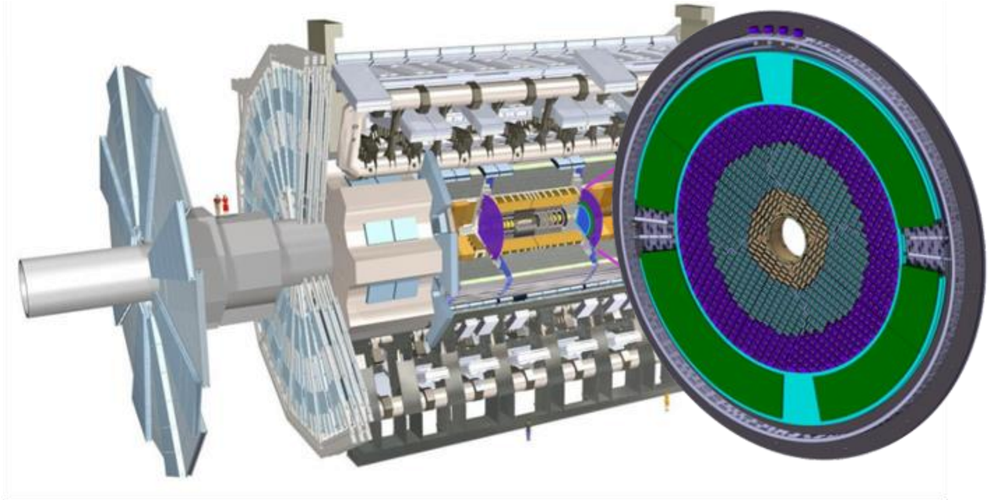


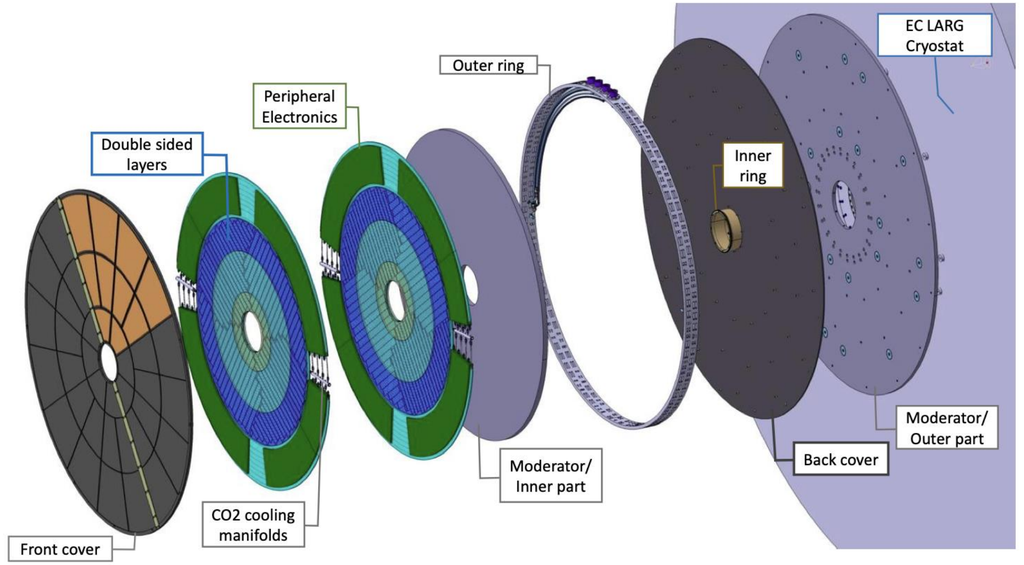




[1704.08666]

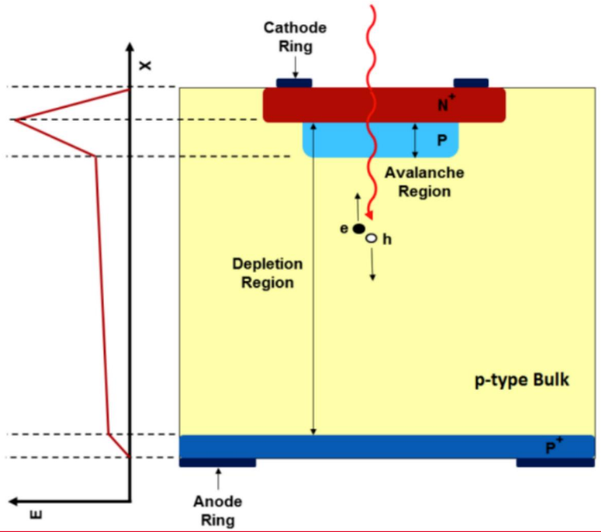
Introduction to High Granularity Timing Detector

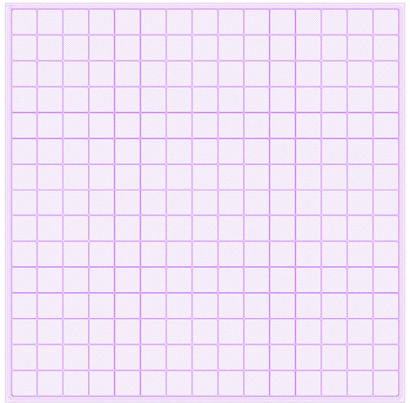




- 2 double sided layers at z=±3500 mm, covering 2.4<|η|<4.0
- Operating temperature -30 ℃
- Time resolution: 35 ps (start) – 70 ps (end)

- Low Gain Avalanche Detector technology is used
- 15x15 pads
- Pad size: 1.3 mmx1.3 mm
- Thickness: 775 μm (physical)/50 μm (active)





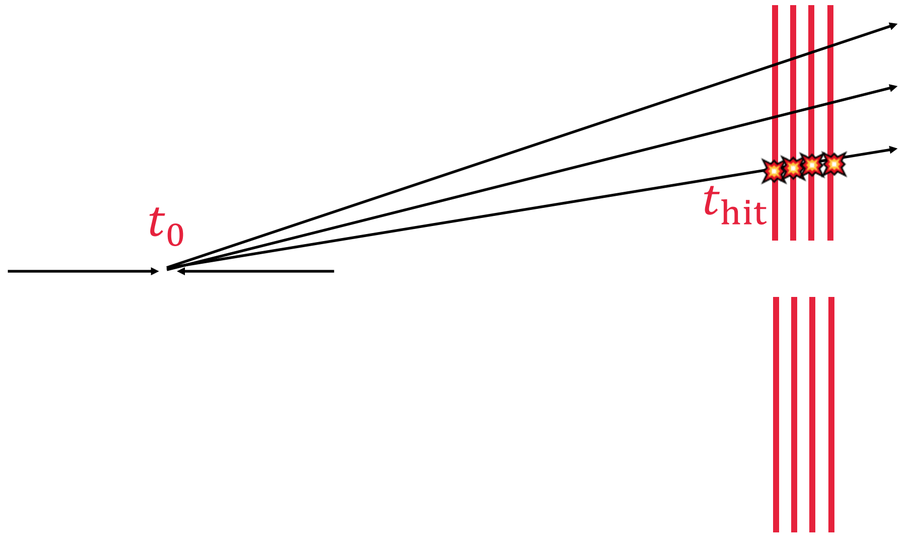
Calibration

t_{hit}

$$\sigma^2_{\mathrm{total}} = \sigma^2_{\mathrm{Landau}} + \sigma^2_{\mathrm{Timewalk}} + \sigma^2_{\mathrm{Jitter}} + \sigma^2_{\mathrm{TDC}} + \sigma^2_{\mathrm{Clock}}$$

1704.08666

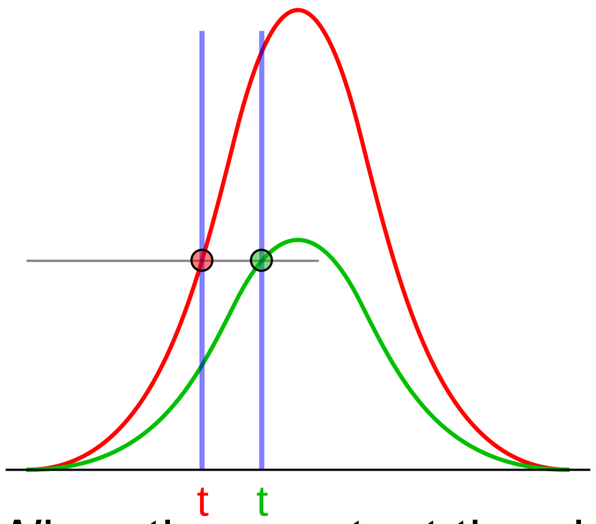
- $\sigma_{\mathrm{Timewalk}}$: the t_{TOA} will depends on the signal amplitude if constant threshold triggering is used, can be corrected using t_{TOT}
- σ_{TDC}: relates to TDC binning and non-linearity, expected to be $\geq 20\ \mathrm{ps}/\sqrt{12}$
- σ_{Clock}: relates to the jitter of the 40MHz clock, expected to be $< 15\ \mathrm{ps}$ after calibration



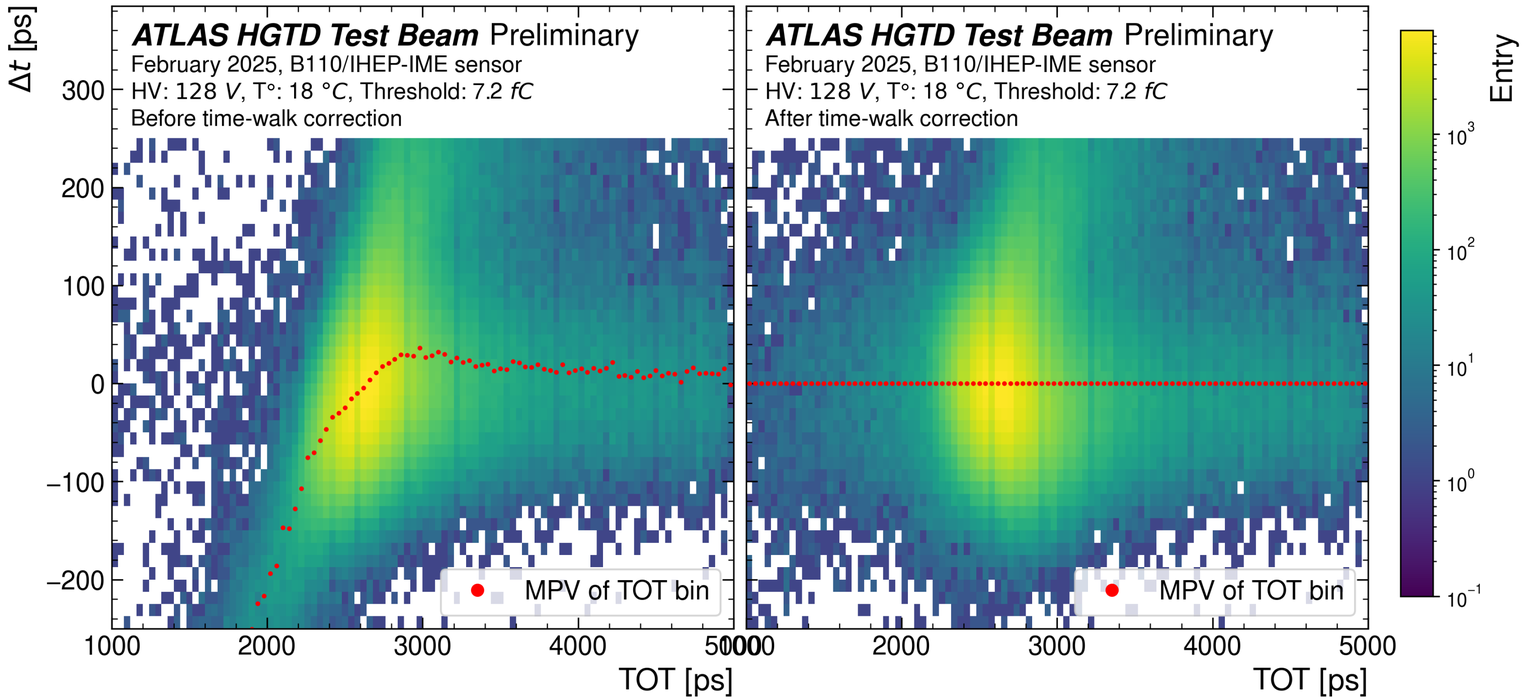
t_0

- Correspond to the bunch crossing time. The different HGTD hits in one event should give the same t_0, which must be calibrated

Time Walk Calibration



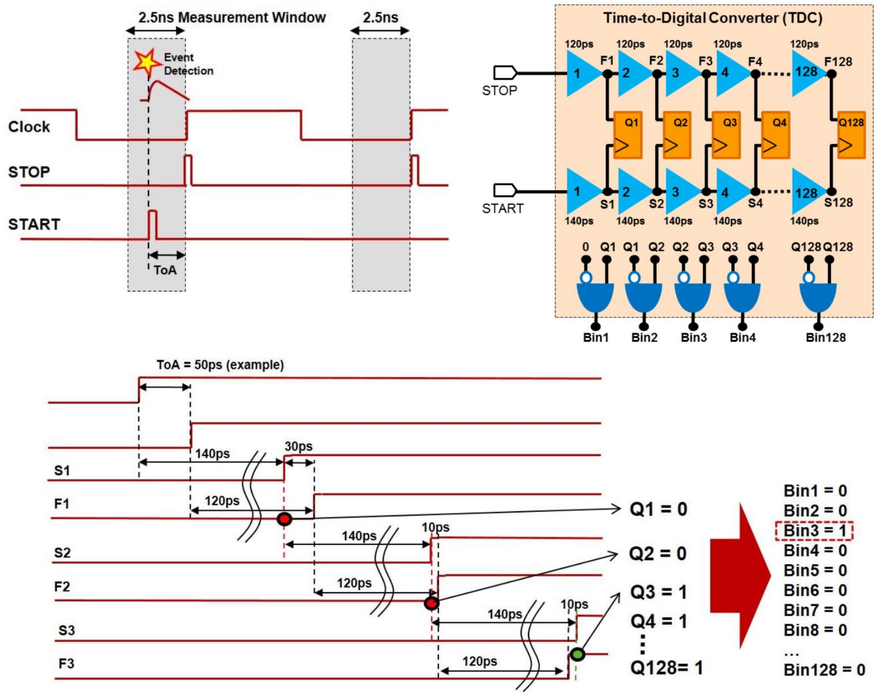
- When the constant threshold is used to determine TOA, the TOA will vary according to the pulse height
- The TOT also correlates with the pulse height, and can be used to correct the time walk effect



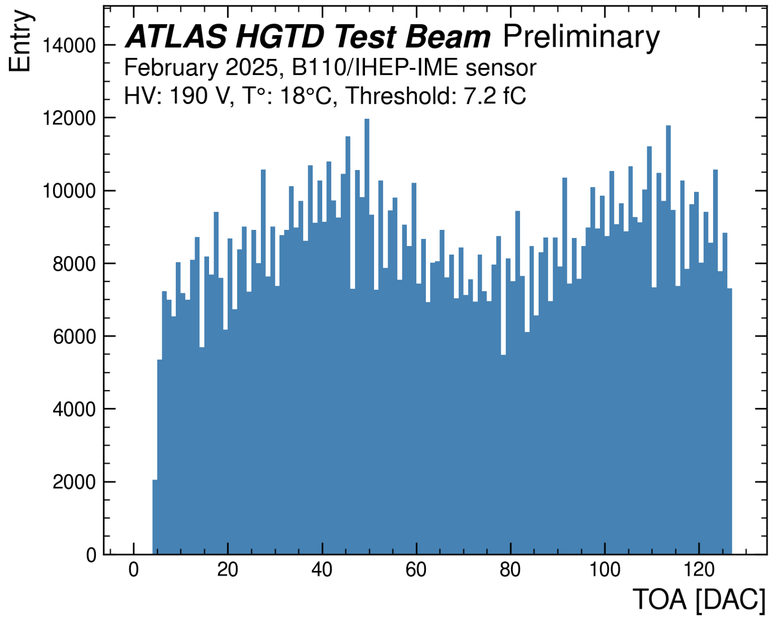
https://twiki.cern.ch/twiki/bin/view/AtlasPublic/HGTDTestBeamALTIROCA

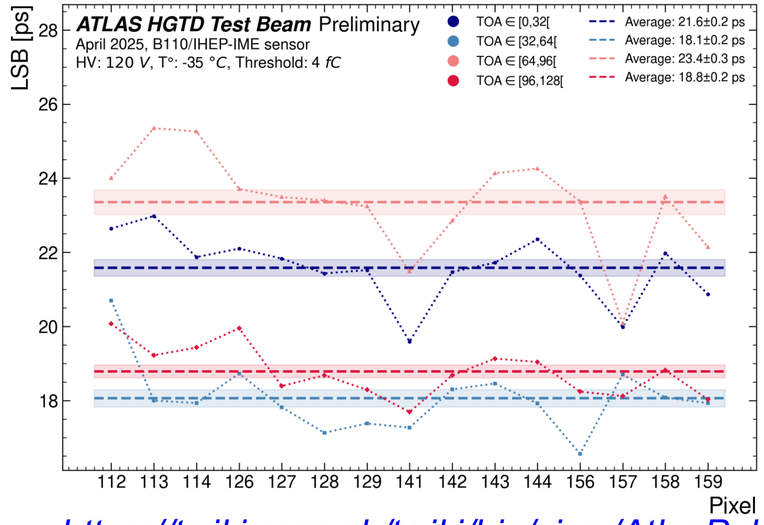
The time walk effect is largely reduced after the correction

TDC Bin Calibration



- Quantization error corresponds to the TDC quantization step size (or LSB, Least Significant Bit)
- Despite the nominal 20 ps LSB, non-linearity has been observed over the 128 TDC bins
- The LSB also depends on the temperature, and possibly the stability of power supply, and has to be calibrated



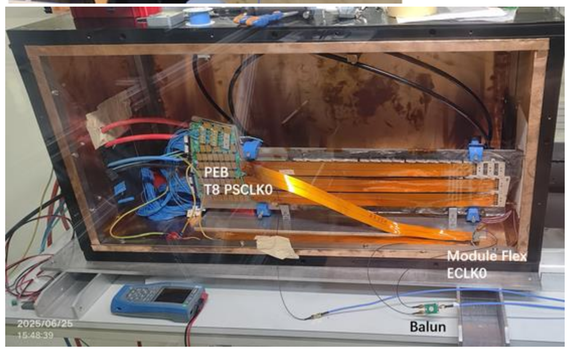


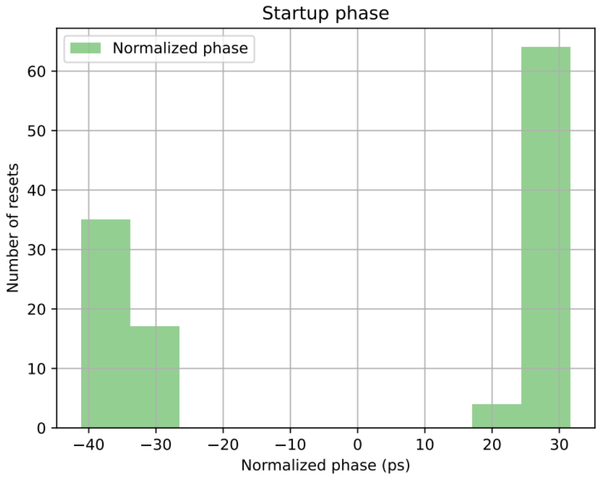
Calibration:

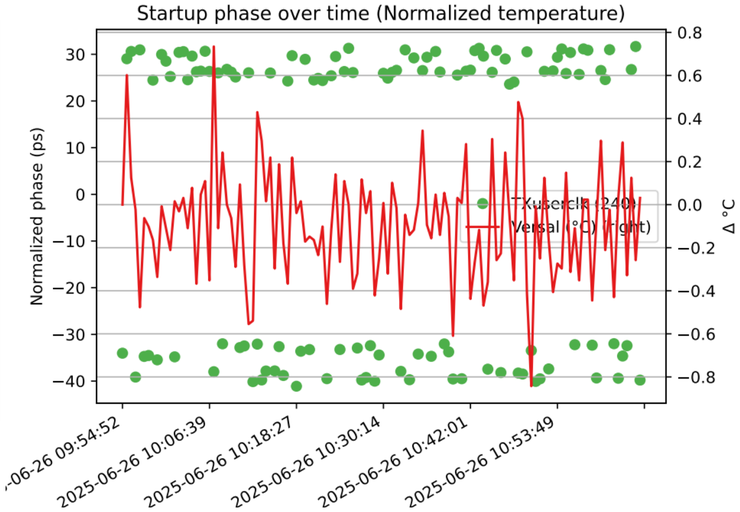
- Internal charge injection in ASIC
- Data-driven calibration using testbeam data

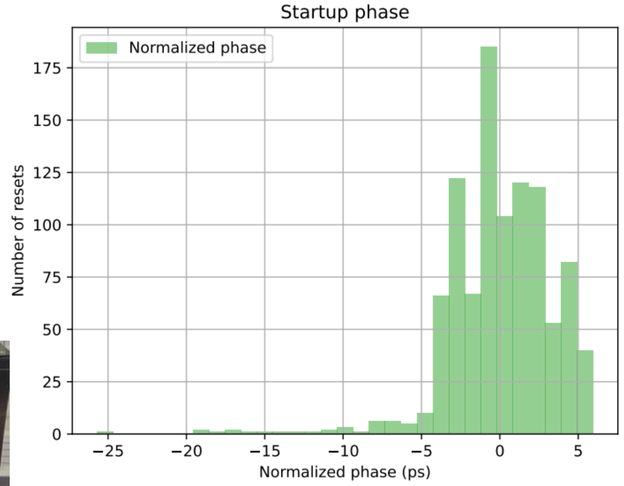
https://twiki.cern.ch/twiki/bin/view/AtlasPublic/HGTDTestBeamALTIROCA

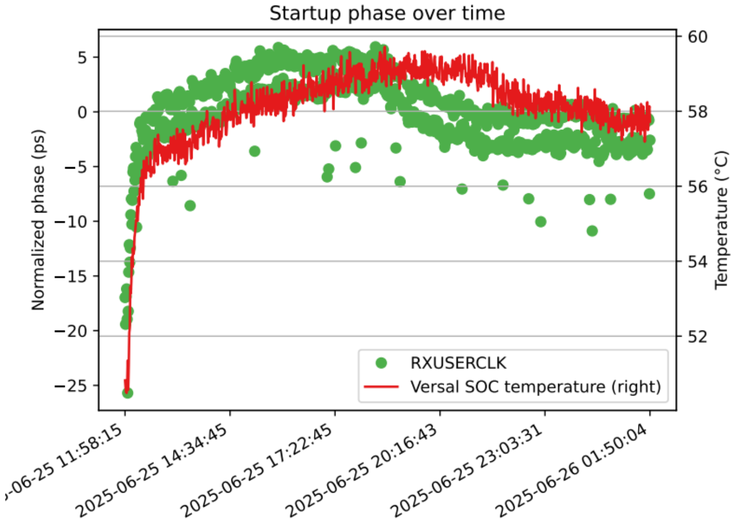
Clock



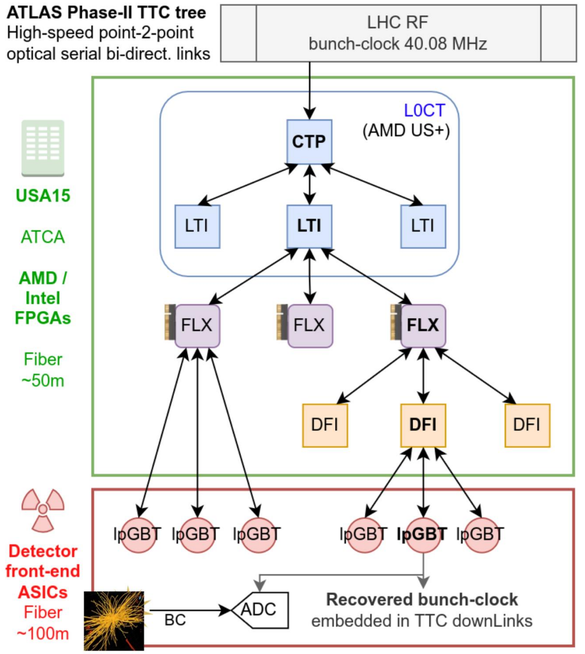








https://jupyter.lhep.Ac.Cn/s/flf2e6phc



CTP: central trigger unit
LTI: local trigger interface

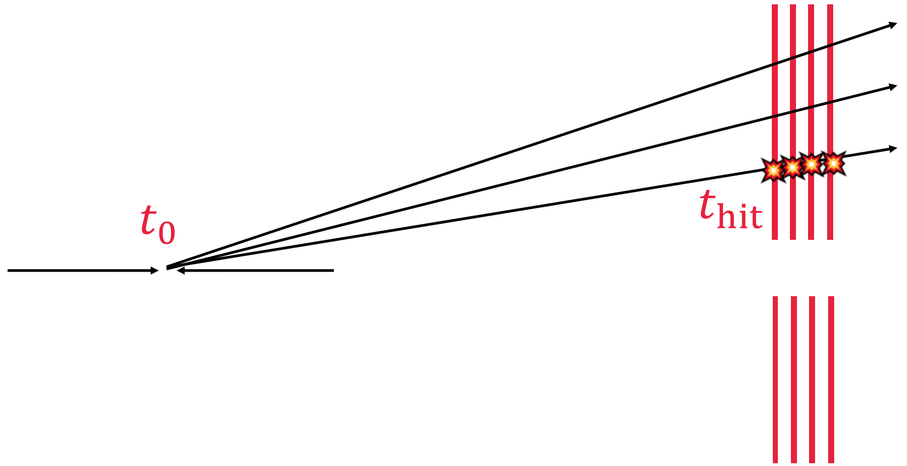
ATL-DAQ-SLIDE-2024-456

LTI→FELIX→VTRx+→lpGBT→Module Flex
Phase difference between LTI and Module Flex

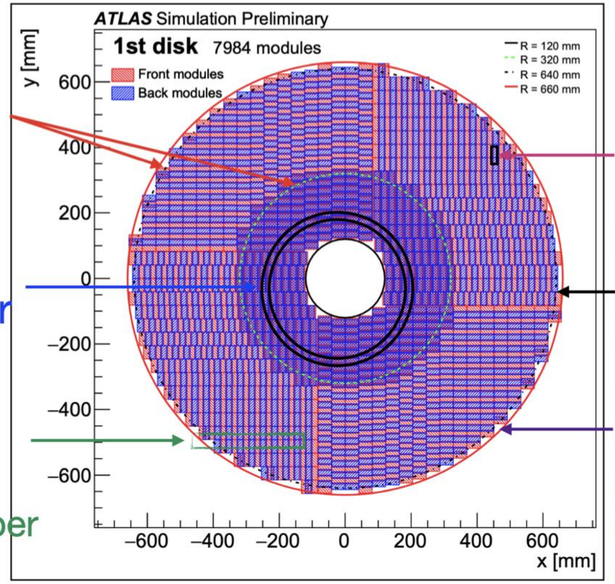
~4 ps clock jitter if the temperature drift effect can be compensated

t_0

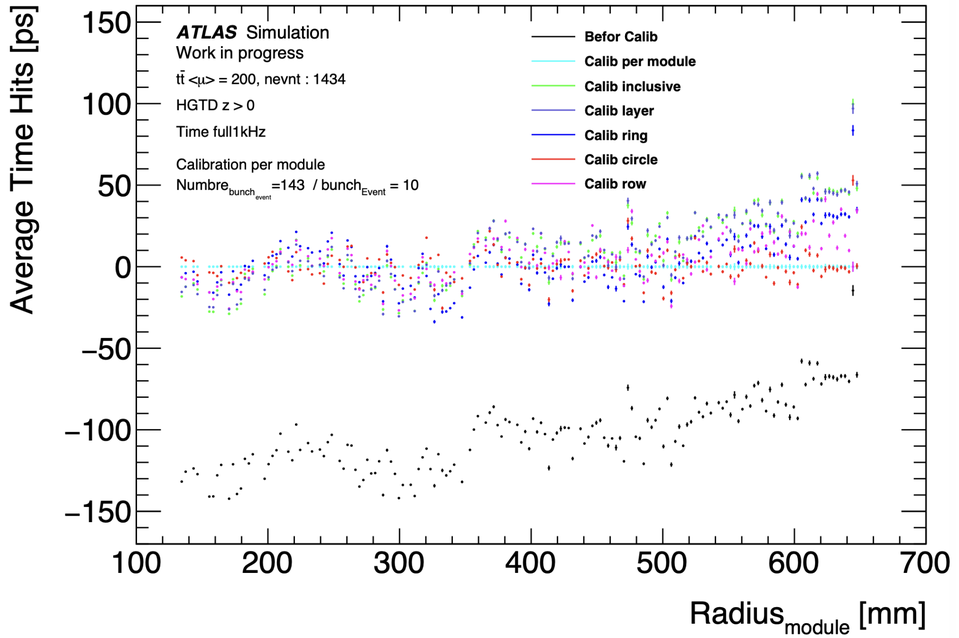
$$t_{\text{calib}}(= t_0) = t_{\text{hits}} - \text{Calibration Constant} = t_{\text{hits}} - \langle t_{\text{hit}} \rangle$$



- **Calib. per ring** : constants calibration is computed per ring, inner and outer.
- **Calib. per circl** : constants calibration per layer and circles defined by dR=40.
- **Calib. per row** : constants computed per layer and per row, as defined by the readout electronics



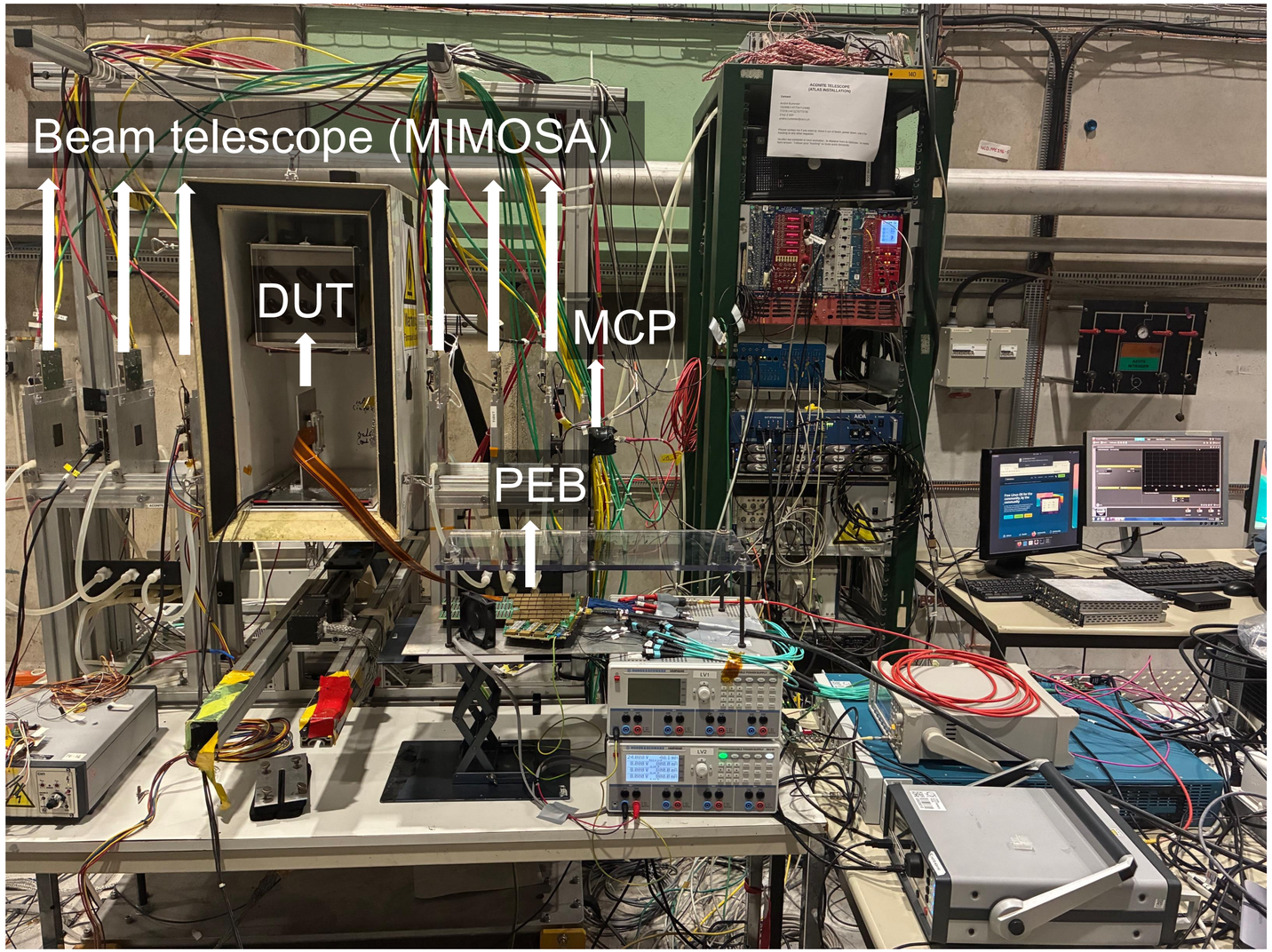
- **Calib. per module** : constants calibration is computed at level of module.
- **Calib. per layer** : constants calibration is computed at level of layer.
- **Calib. per inclusive** : constants calibration is computed at level of 2 disks.

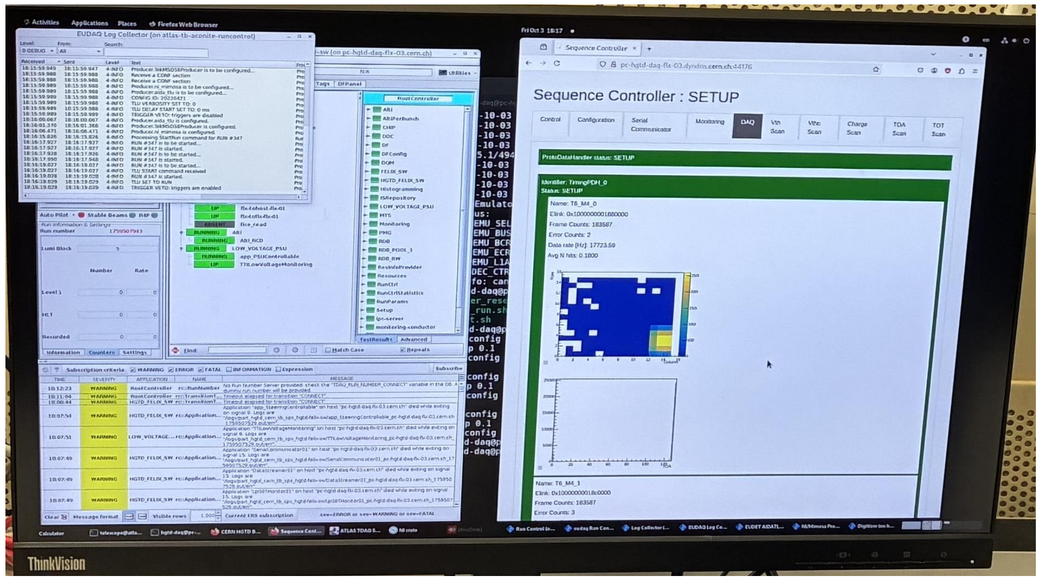


https://conferences.slac.stanford.edu/sites/default/files/2023-09/Poster_01_Abdellah%20Tnourji.pdf

The ToF effect can be compensated using the calibration per module method

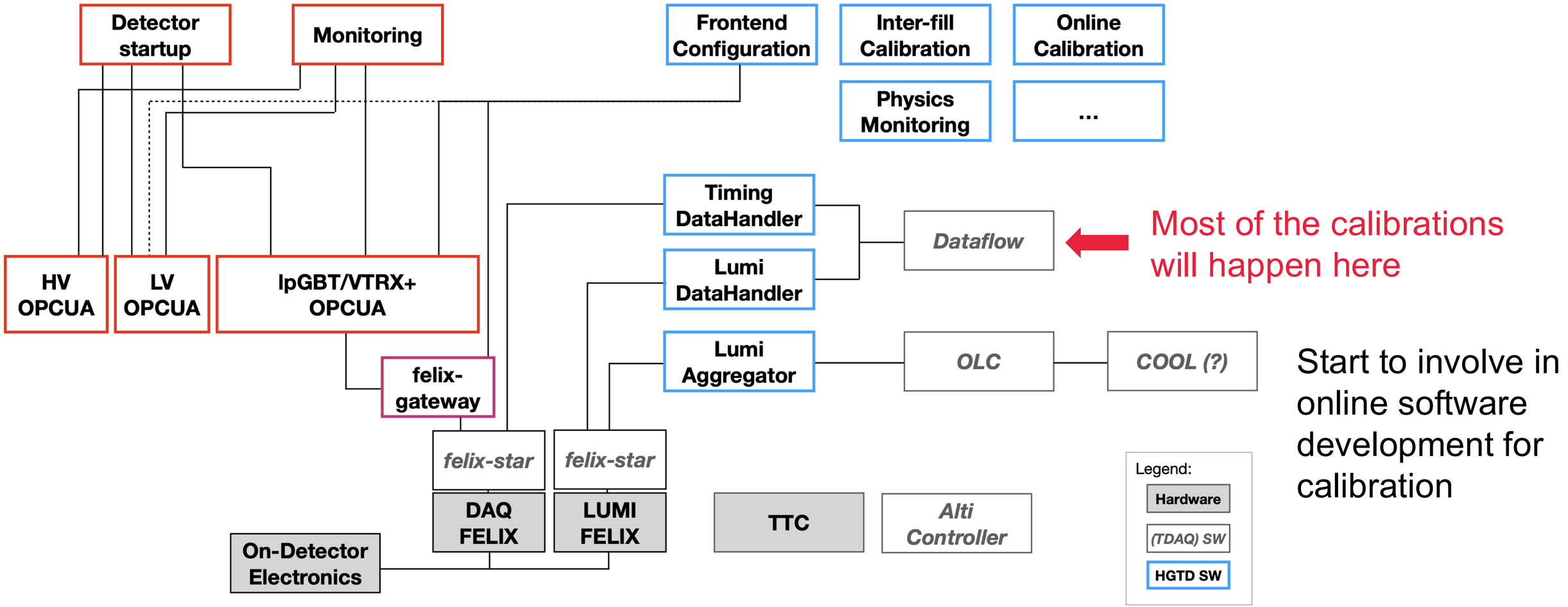
HGTD Testbeam October 2025





The first time reading out data using the HGTD online software through the Peripheral Electronics Board (PEB) and FELIX card

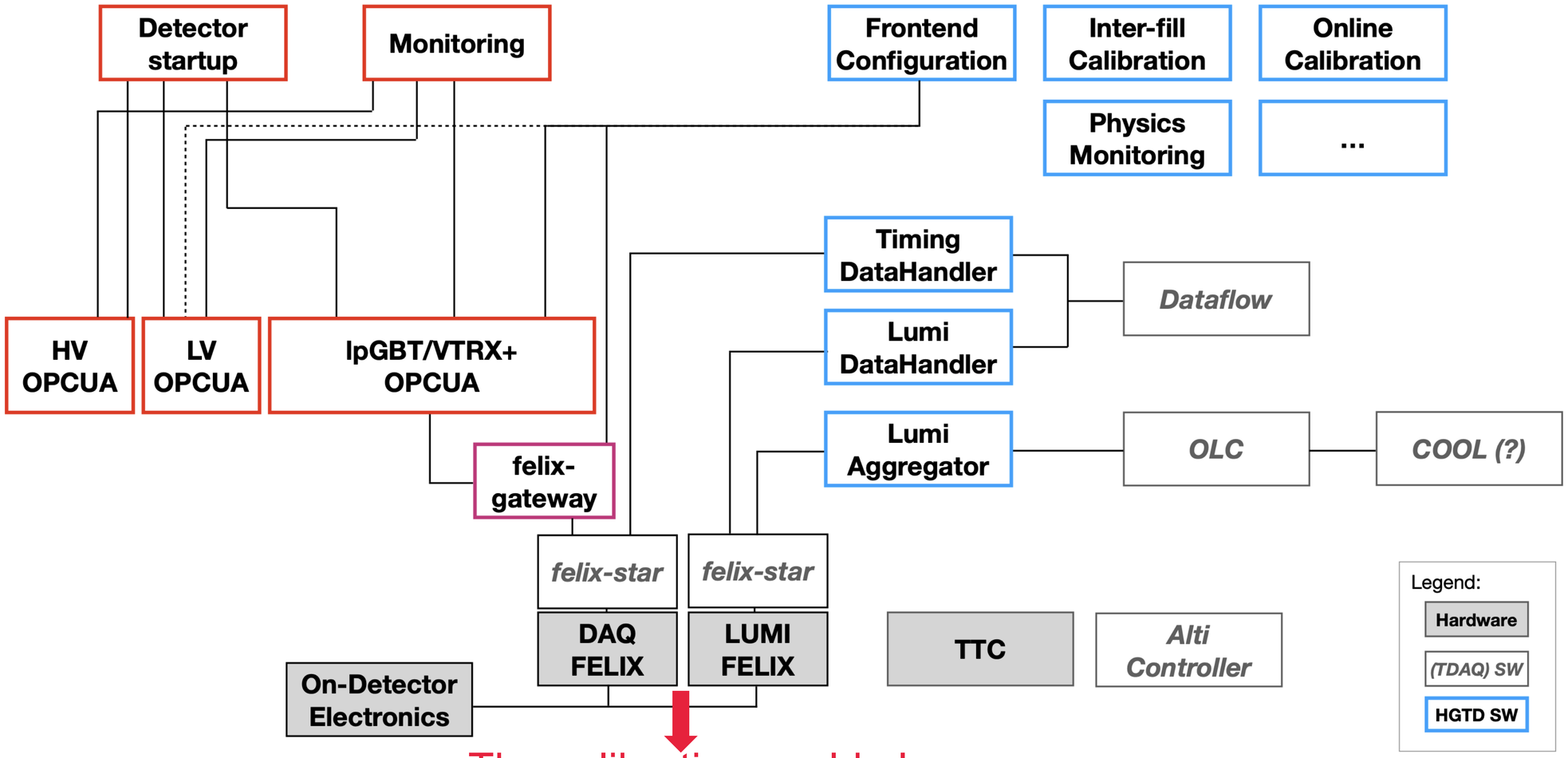
Calibration on HGTD Online Software



Most of the calibrations will happen here

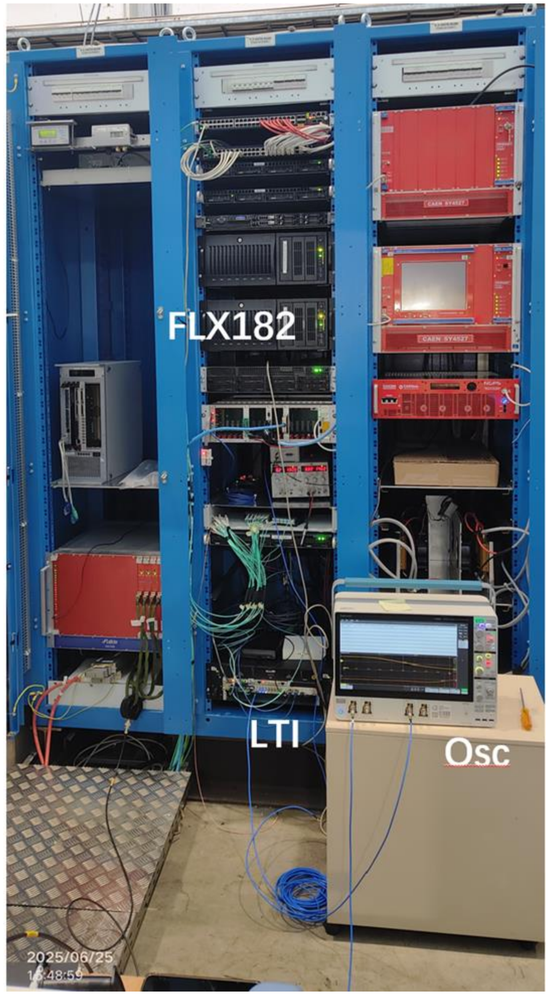
Start to involve in online software development for calibration

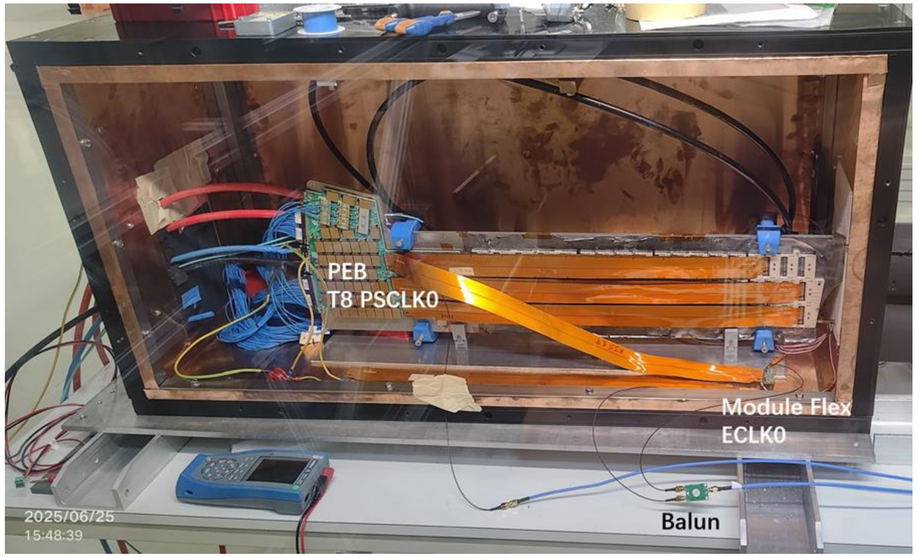
Calibration on FPGA



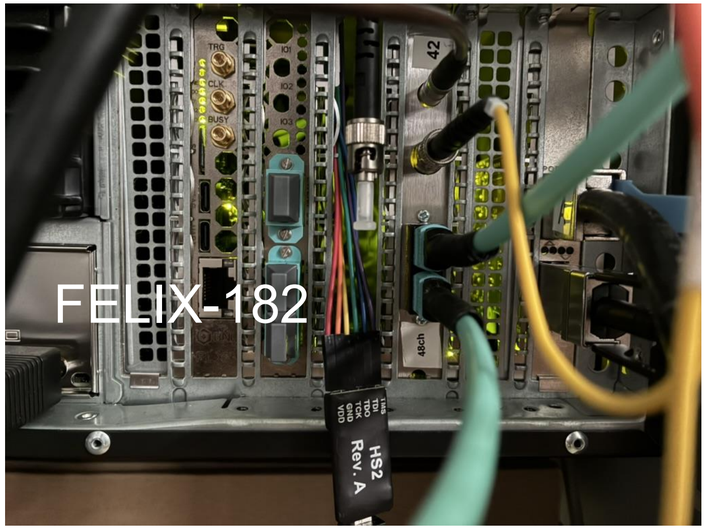
The calibration could also be done here, for R&D

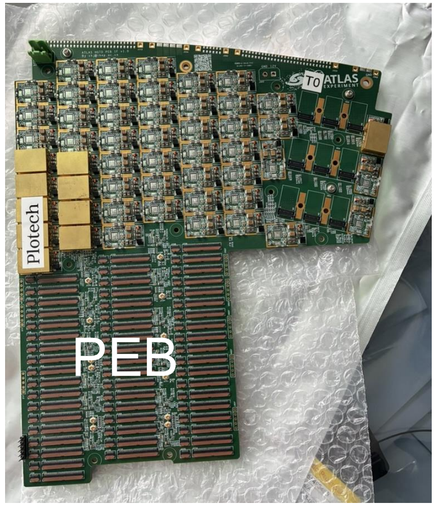
Setup in Nijmegen | Replicate the setup at CERN

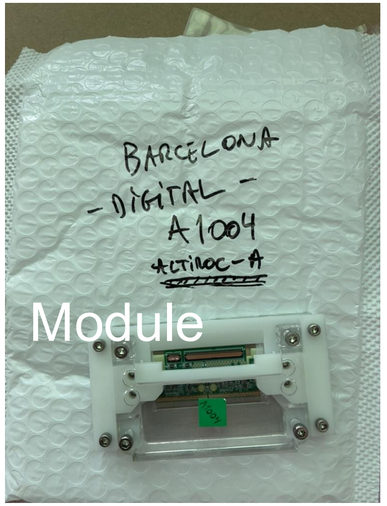




CERN setup







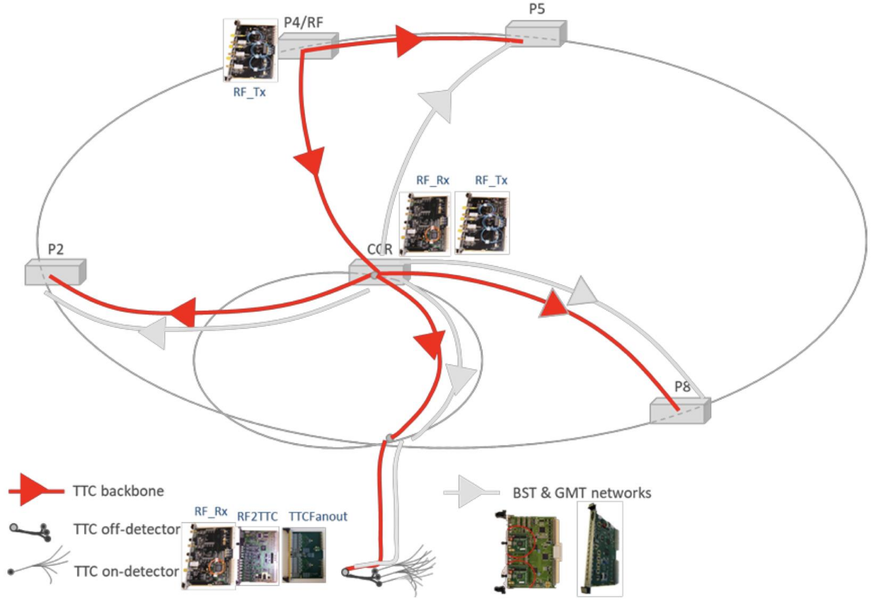
Plan

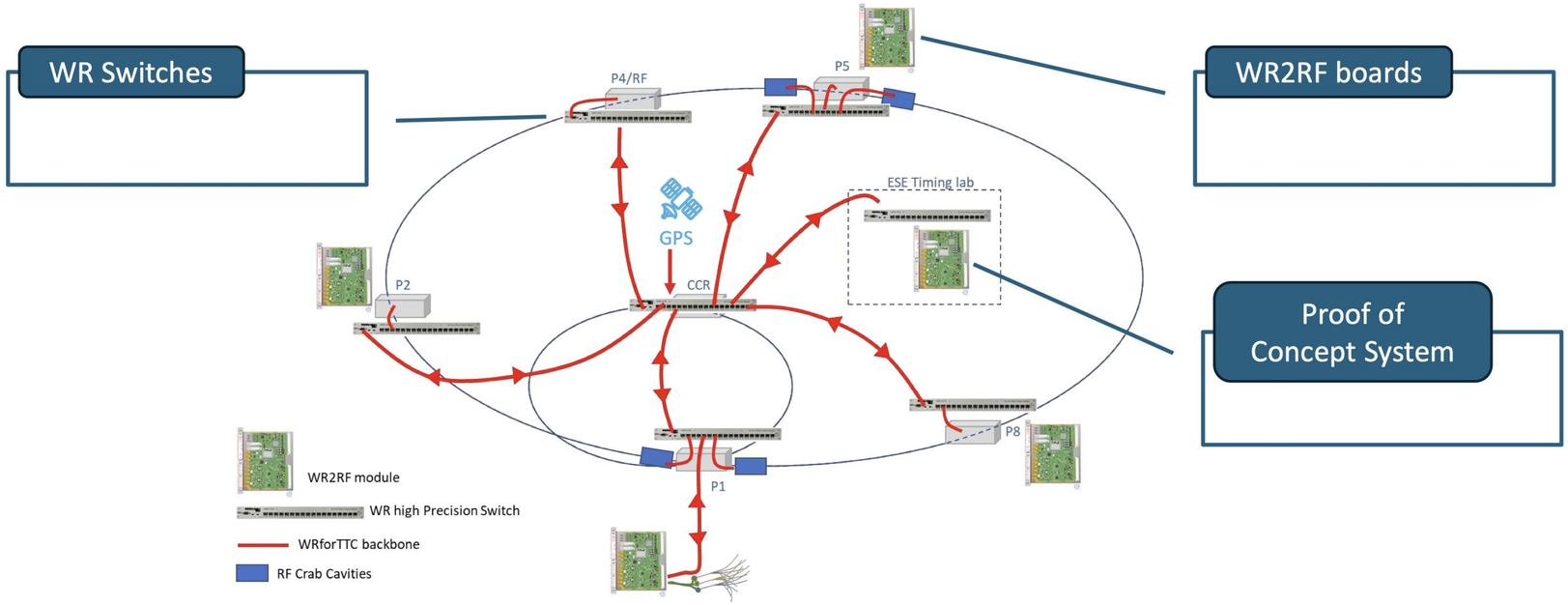
- Having a proper HGTD DAQ setup at Nijmegen to measure clock and timing, possibly also a beta source setup
- Analyse testbeam data to have better understanding of the module performance and the corresponding calibrations
- Involve in online software development and discover the feasibility of implementing the different calibration algorithms
- Once the calibration algorithms on the online software are in good shape, consider the possibility of implementing them using FELIX

Thank you

Backup

Backup


P4/RF
P5
RF_Tx
RF_Rx
RF_Tx
P2
CCR
P8
TTC backbone
TTC off-detector
TTC on-detector
RF_Rx
RF2TTC
TTCFanout
BST & GMT networks


WR Switches
WR2RF boards
P4/RF
P5
ESE Timing lab
GPS
P2
CCR
P8
P1
Proof of Concept System
WR2RF module
WR high Precision Switch
WRforTTC backbone
RF Crab Cavities