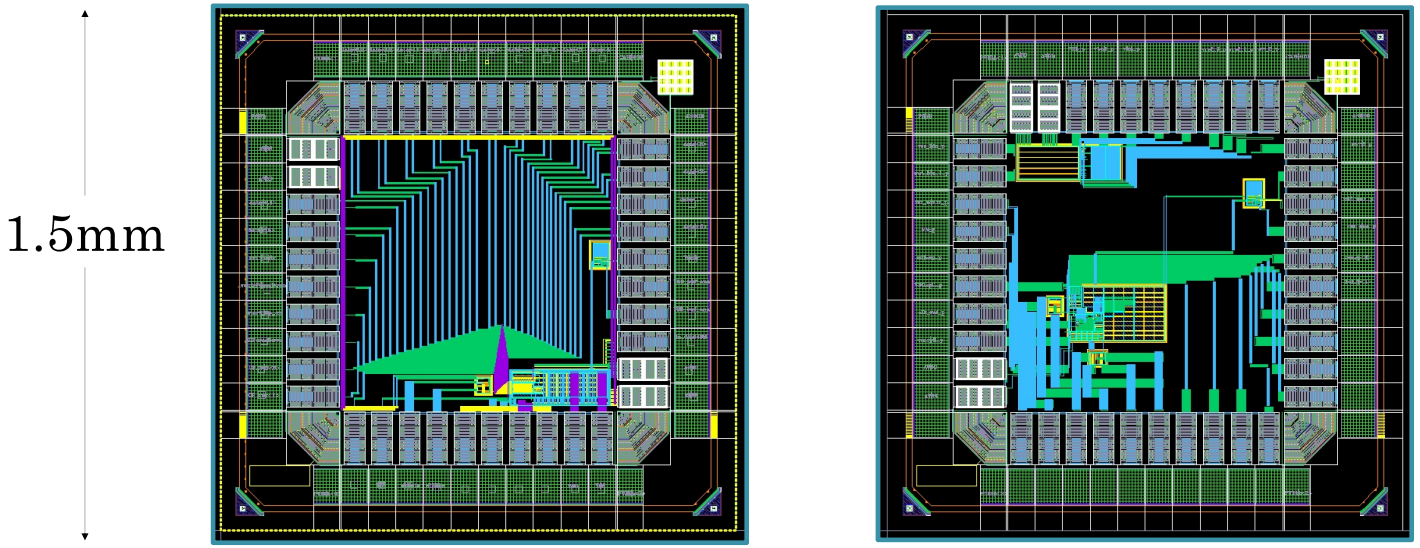
Development of a 10.24Gbps Data Serializer Integrated Circuit for the readout of the ALICE ITS3 detector

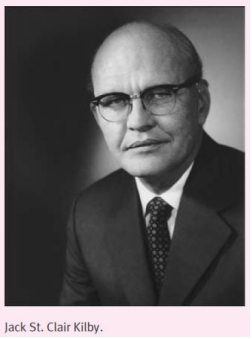


Vladimir Gromov
Nikhef, Amsterdam, the Netherlands

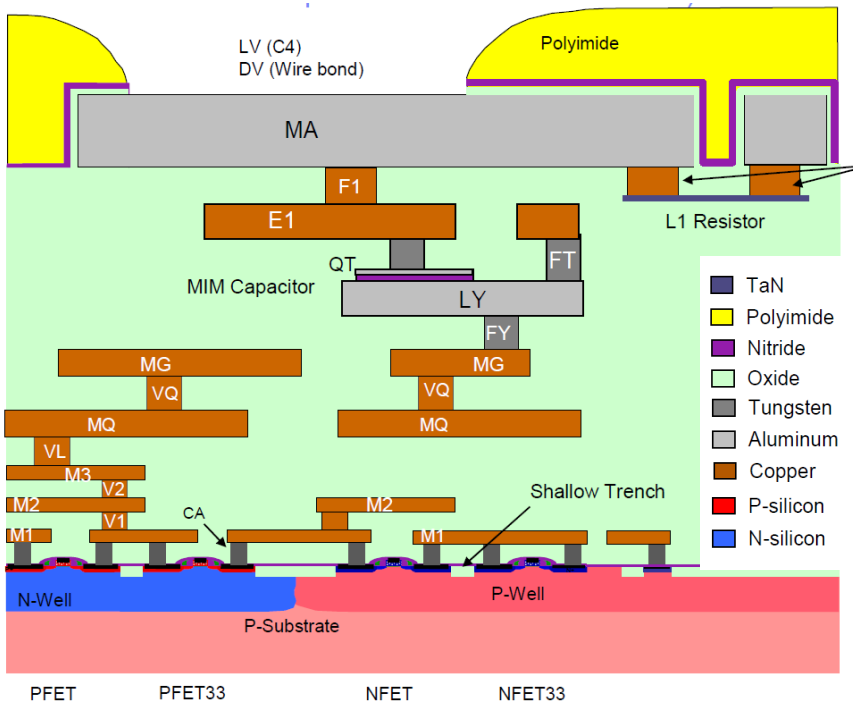
May 13, 2024

Integrated Circuit technology

Jack Kilby:
the Nobel Prize
in Physics 2000



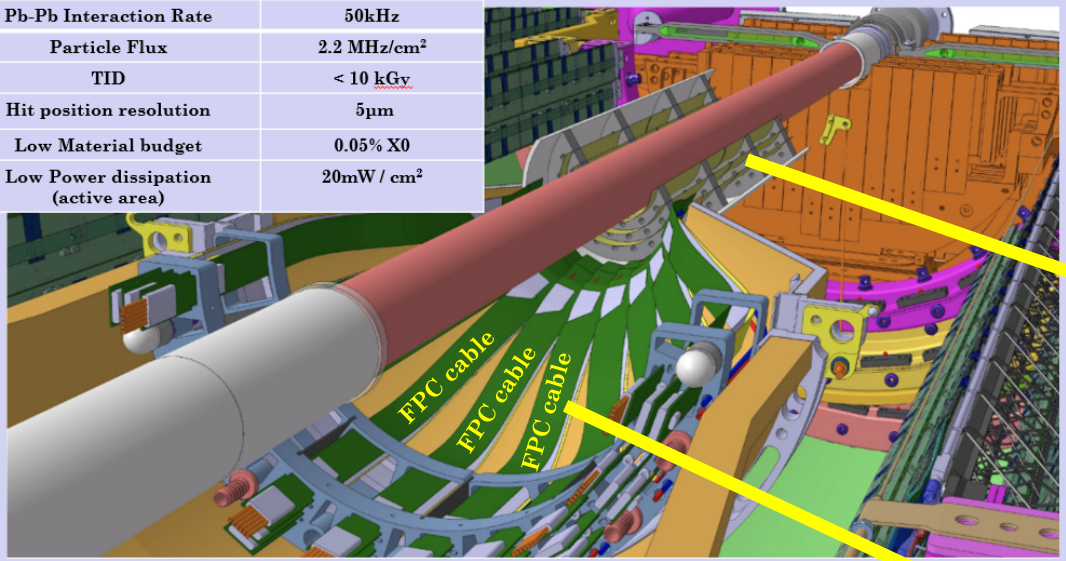
- large-scale module (system-on-chip)
- miniaturization
- fast operation (less parasitic caps)
- cost effective



Vertex Detector in ALICE Inner Tracking System 3 (ITS3)

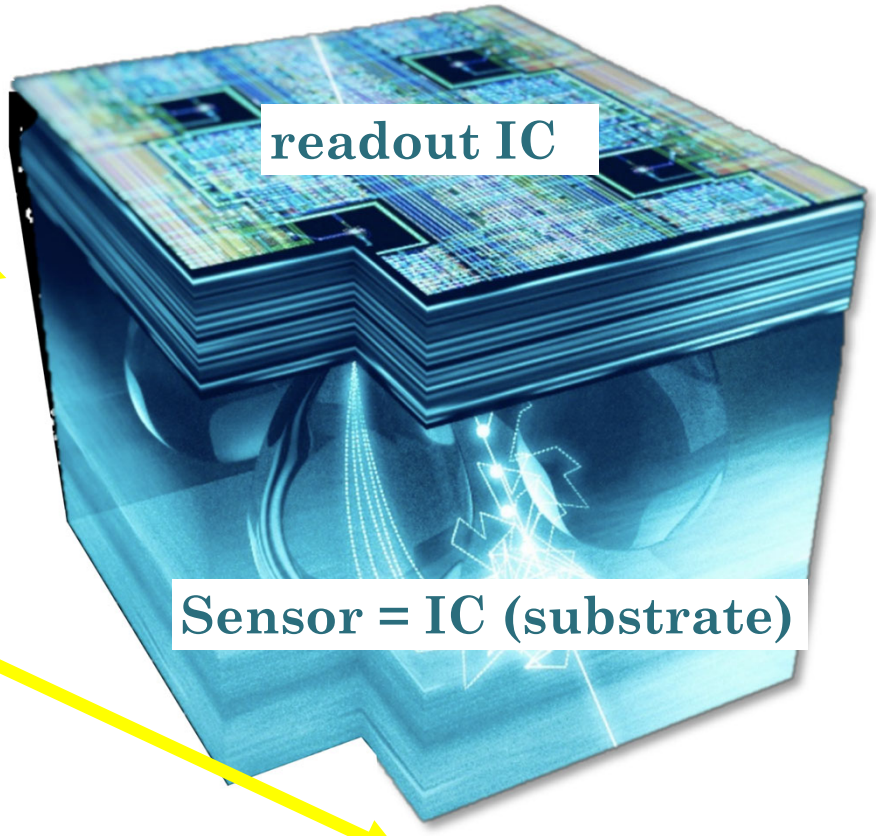
ITS 3 layout

Pb-Pb Interaction Rate	50kHz
Particle Flux	2.2 MHz/cm^2
TID	< 10 kGy
Hit position resolution	5μm
Low Material budget	0.05% X0
Low Power dissipation (active area)	20mW / cm^2



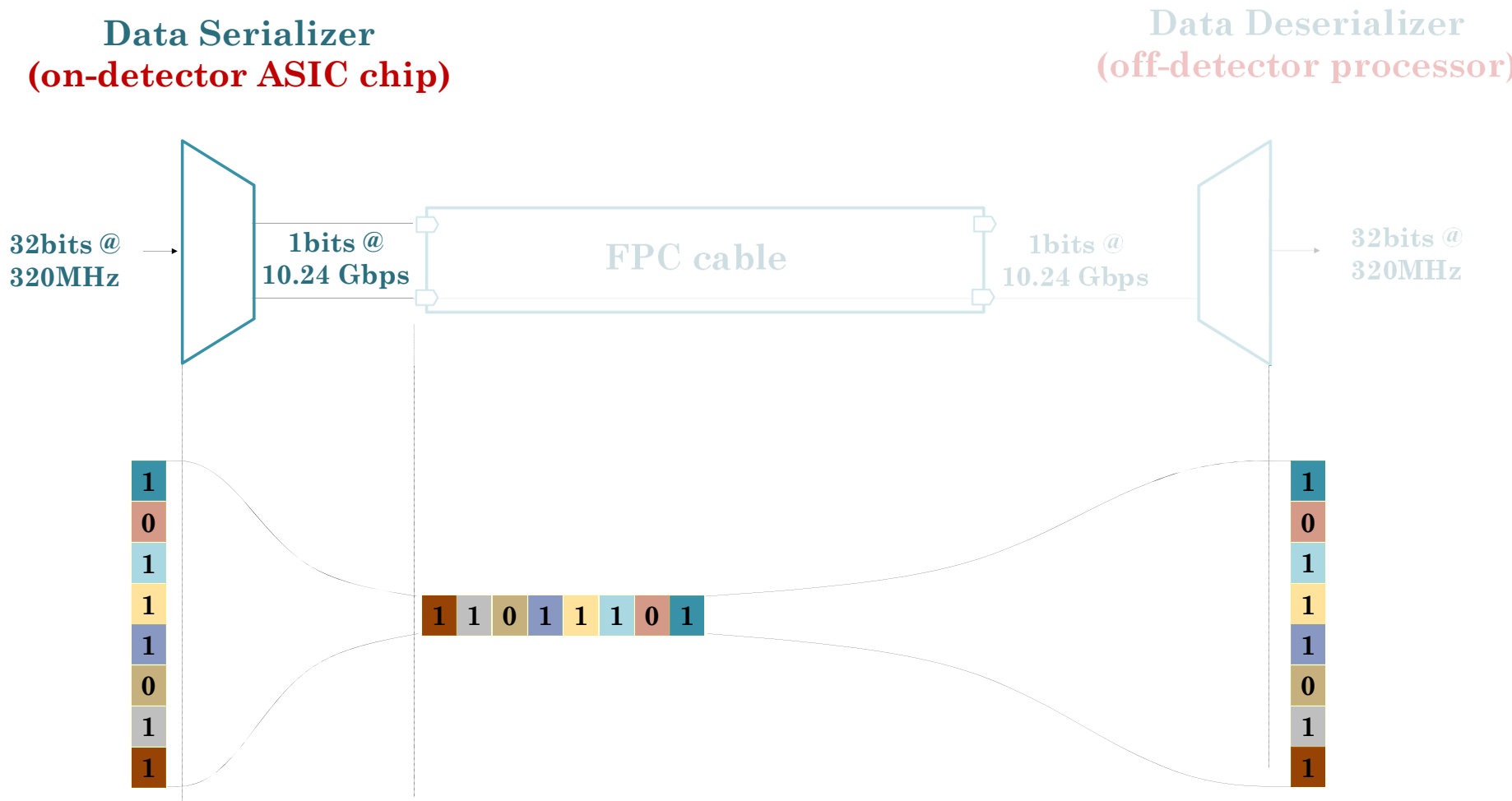
- Vertex detector in 65nm MAPS technology (pixel size ~20μm)
- 3 curved single-die detector layers (radius 18/24/30 mm)
- each sensor die is a 28cm long (wafer-scale) ASIC chip thinned to 50μm

MAPS: Monolithic active pixel sensors
(TPSCo 65 nm CMOS technology)



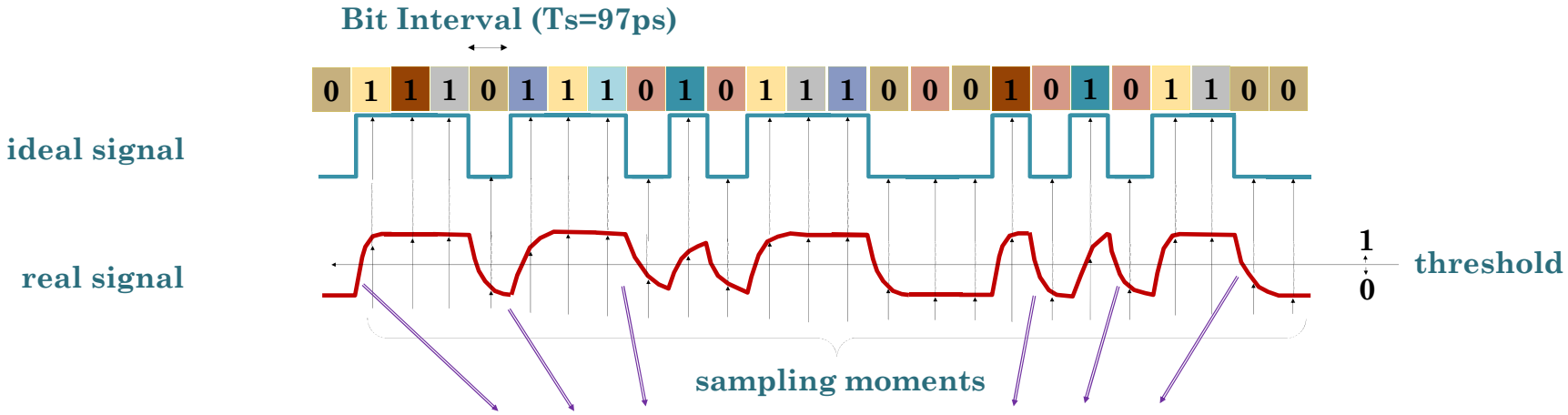
- the Flexible Printed Circuit (FPC) cable will be used to transmit the data from the detector IC to a rate up to 10Gbps

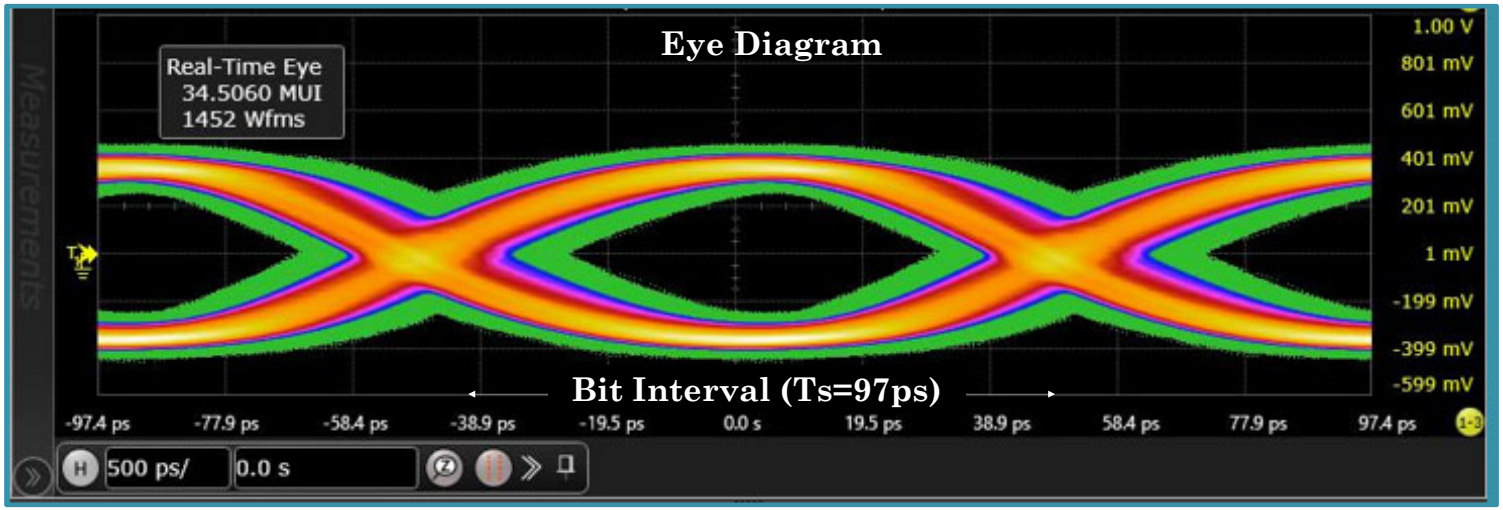
A 10.24Gbps Data Transmission link in ITS3



- data transmission over a single-bit cable is required to minimize the number of the interconnects between the on-detector ASIC chip and the off-detector data processor

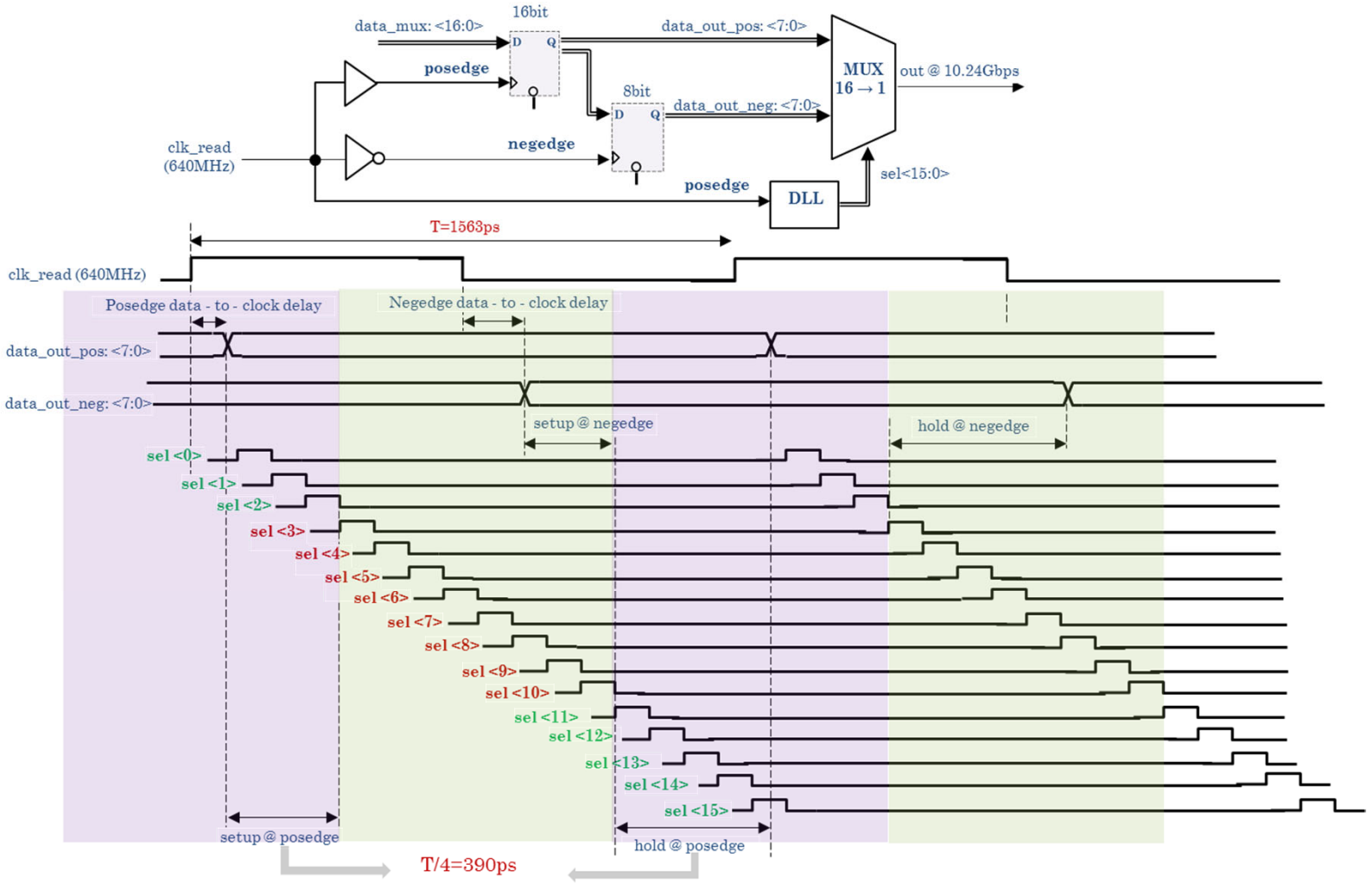
Quality of a 10.24Gbps Data Transmission





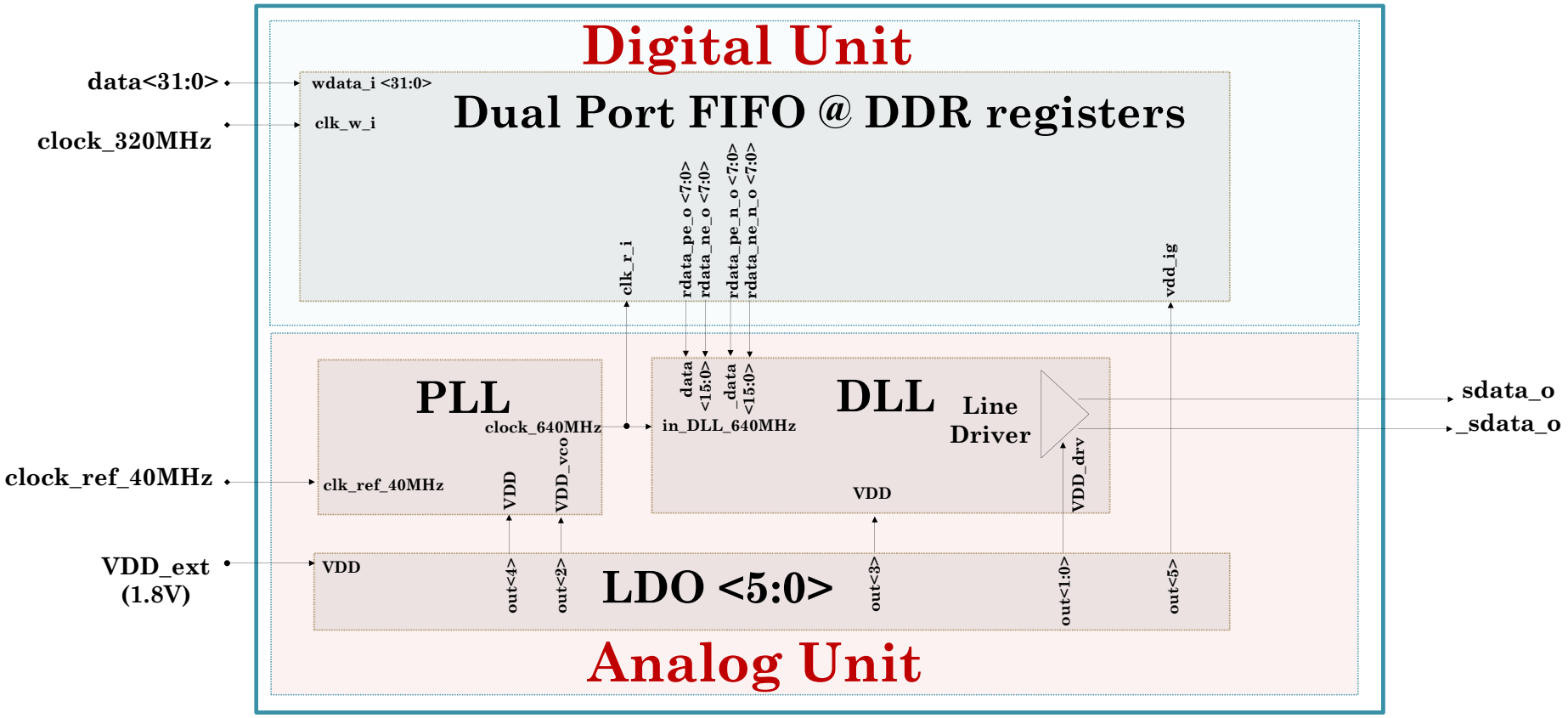
- the bit error occurs when the sampled value does not match to the origin value
- the wider the opening of the Eye Diagram the lower the bit-error rate (BER)

1/16-Rate Multiplexer-based architecture of the Data Serializer



➢ **a 25ps precision of the bit-interval definition is required (selection signal generated inside the serializer)**

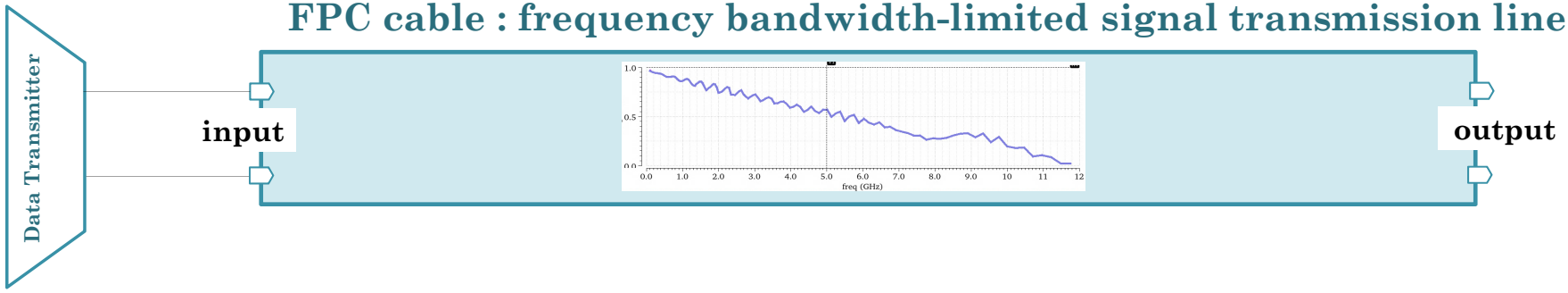
GWT-PSI: a 10.24Gbps Data Serializer and Wireline Transmitter



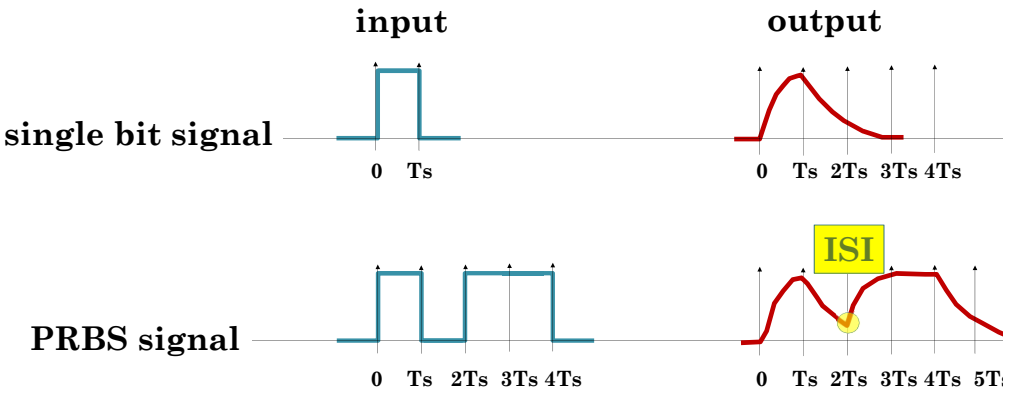
- the Phase-Locked Loop (PLL) generates a low-jitter (<5ps rms) clock (640MHz)
- the Multi-Phase Delay-Locked Loop (DLL) generate a 97ps-spaced selection signal for the 16-to-1 multiplexer
- the built-in voltage regulator (LDO) generate clean (ripple-free) power supply voltage to avoid the bit-interval distortion

Inter-Symbol Interference (ISI) noise mitigation

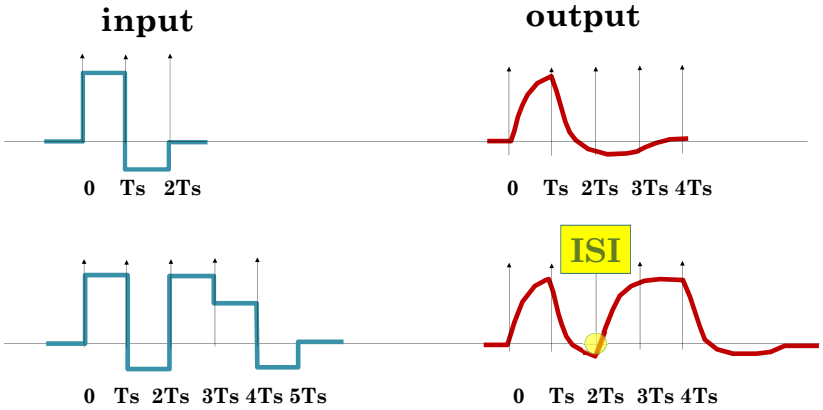
FPC cable : frequency bandwidth-limited signal transmission line



ISI @ NO signal pre-emphasis



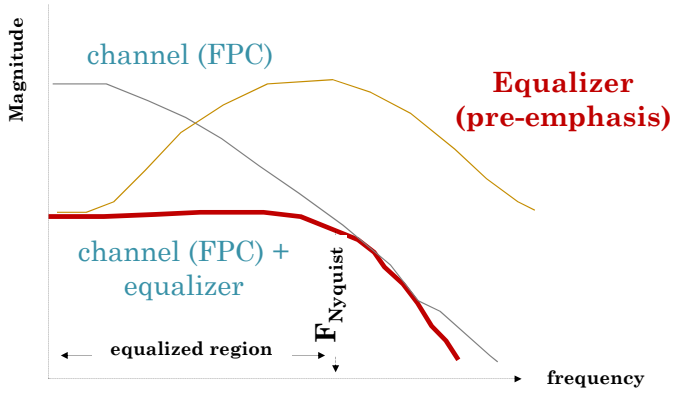
ISI @ WITH signal pre-emphasis



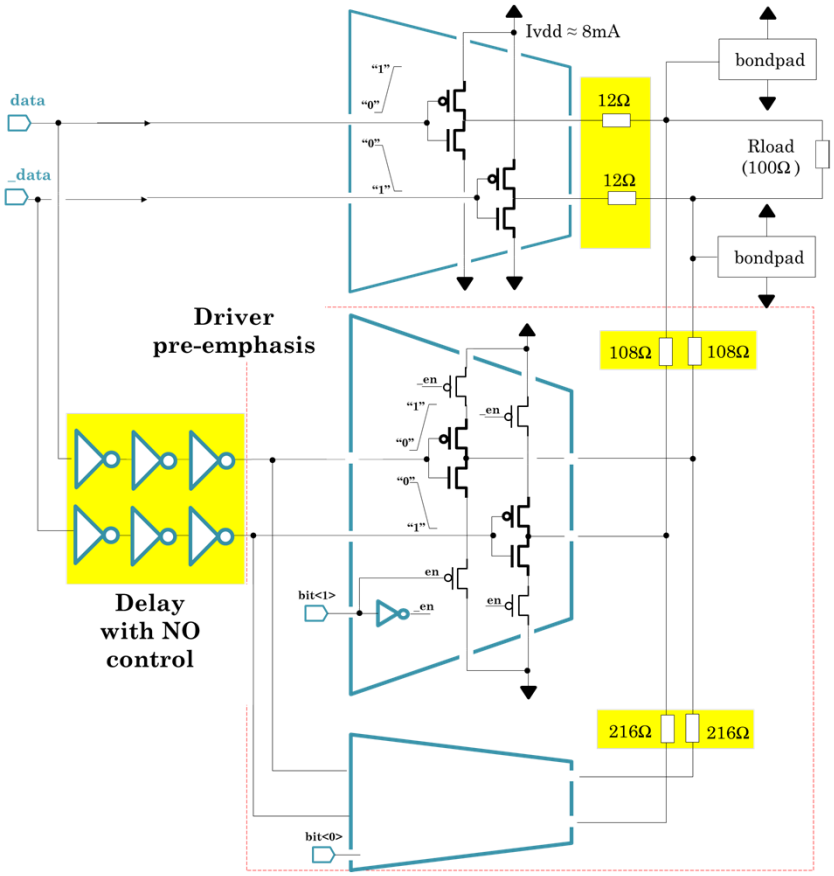
- the shape of the transmitted signal gets distorted due to the limited bandwidth of the FPC cable
- the distortions (after-pulsing) will cause the inter-symbol interference acting as an additional noise source
- the ISI noise can be mitigated by the signal pre-emphasis (pre-distortions) in the transmitter circuit

2-tab signal pre-emphasis in the Transmitter

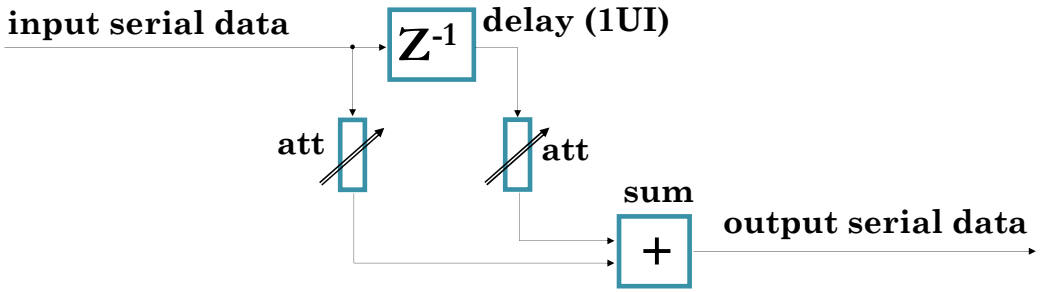
Frequency response equalization



Block diagram of the Transmitter



Feed-Forward Equalizer



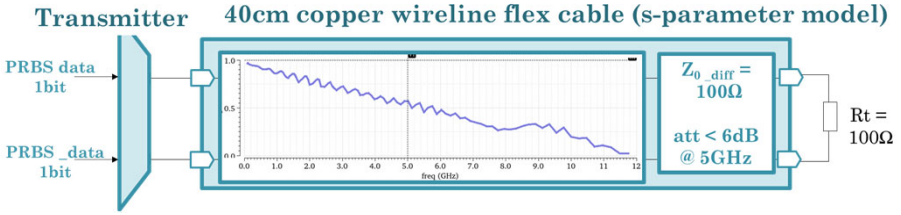
➢ **inter-symbol Feed-Forward Equalizer based on FIR (Finite-impulse Response) filter is the most common approach to implement the pre-emphasis in the signal transmitter**

Data transmission link: effect of the pre-emphasis

technology: TowerJazz 65nm CMOS, lib: /icwork/vgromov/ALICE_ITS3/analog/ITS3, test bench : tb_182 lib:ITS3, **cell: Driver_19_VG = NO delay control , lib:ITS3 , caliber_R_C_CC_lim_23_02_2024**

Test bench

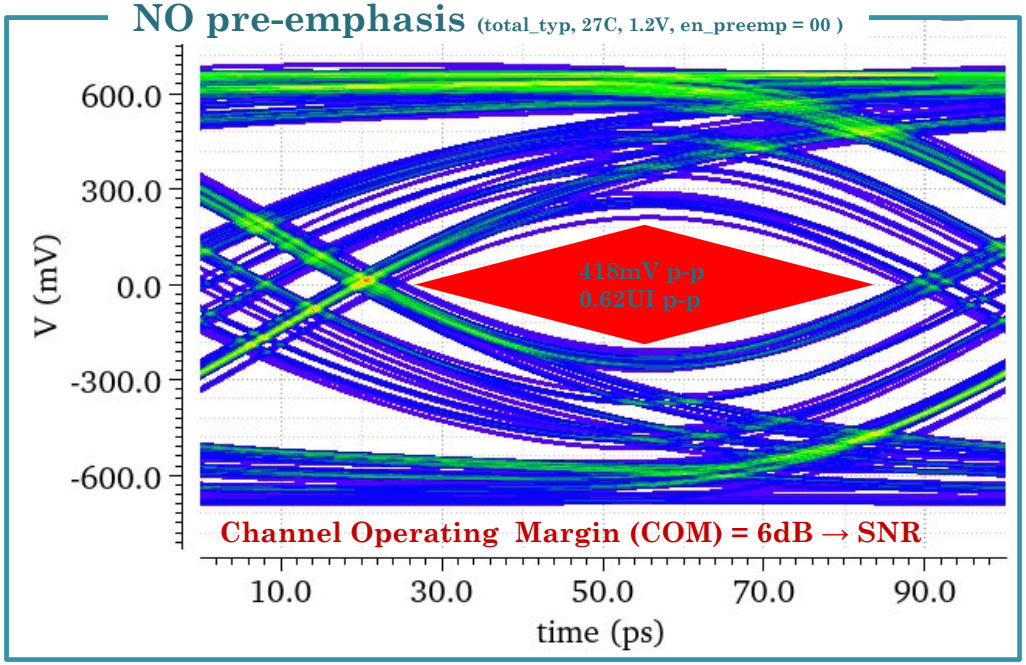
I_{VDD} = 12.7mA @ NO-pre-emphasis (11.5mA @ main driver , 1.5mA @ pre-emphasis driver
I_{VDD} = 22.8mA @ NO-pre-emphasis (12mA @ main driver , 10.5mA @ pre-emphasis driver



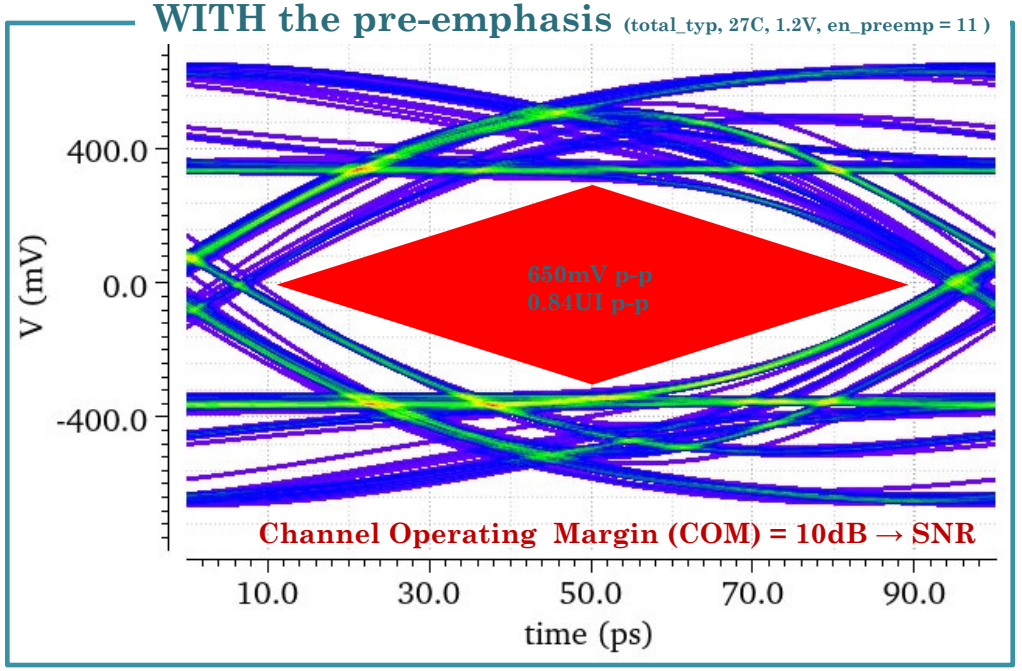
FLEX: ER2_V3_150um-Thick_200um-Lines_full_35cm.S64P
ZIF connector: FH34SRJ_GSSGSSG_Top_contact_Diff100ohm.s8p

Eye Diagrams @ receiver (diff.)

NO pre-emphasis (total_typ, 27C, 1.2V, en_preemp = 00)

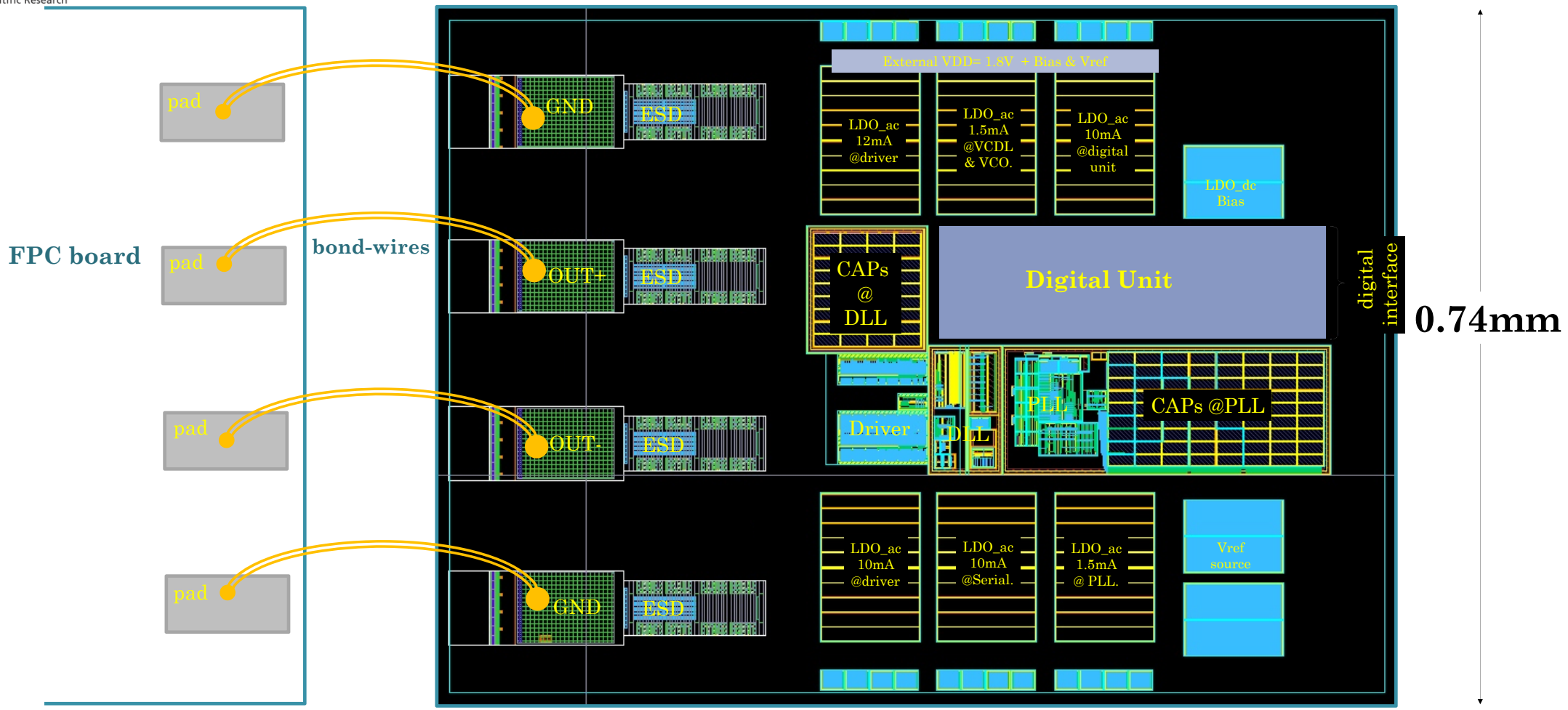


WITH the pre-emphasis (total_typ, 27C, 1.2V, en_preemp = 11)



➢ **the pre-emphasis improves the quality of the Data Transmission Link (opening of the Eye Diagram)**

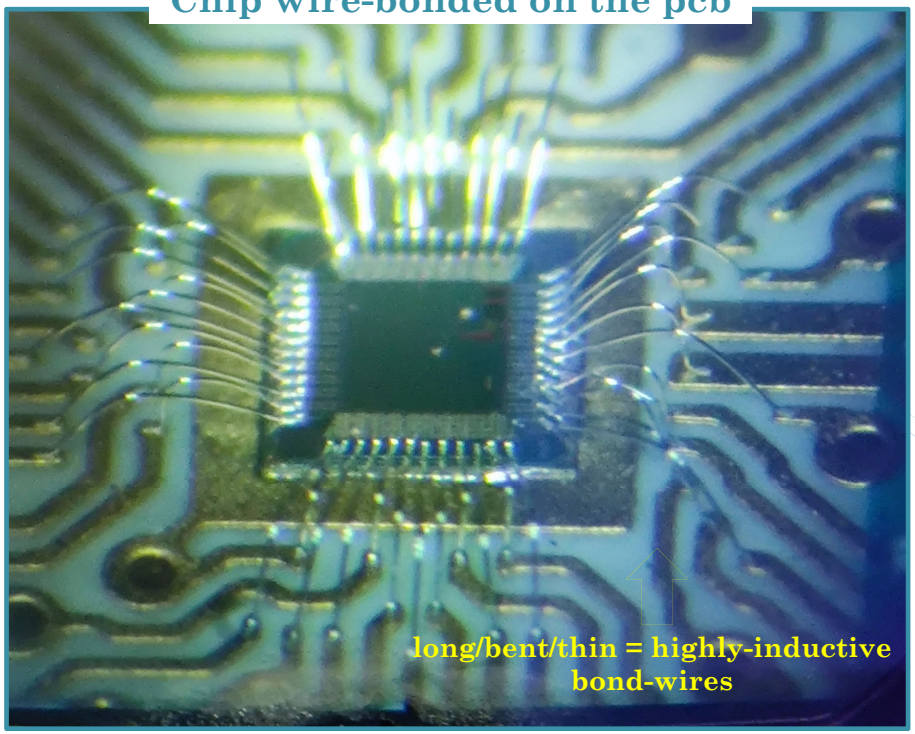
Layout of the GWT-PSI block

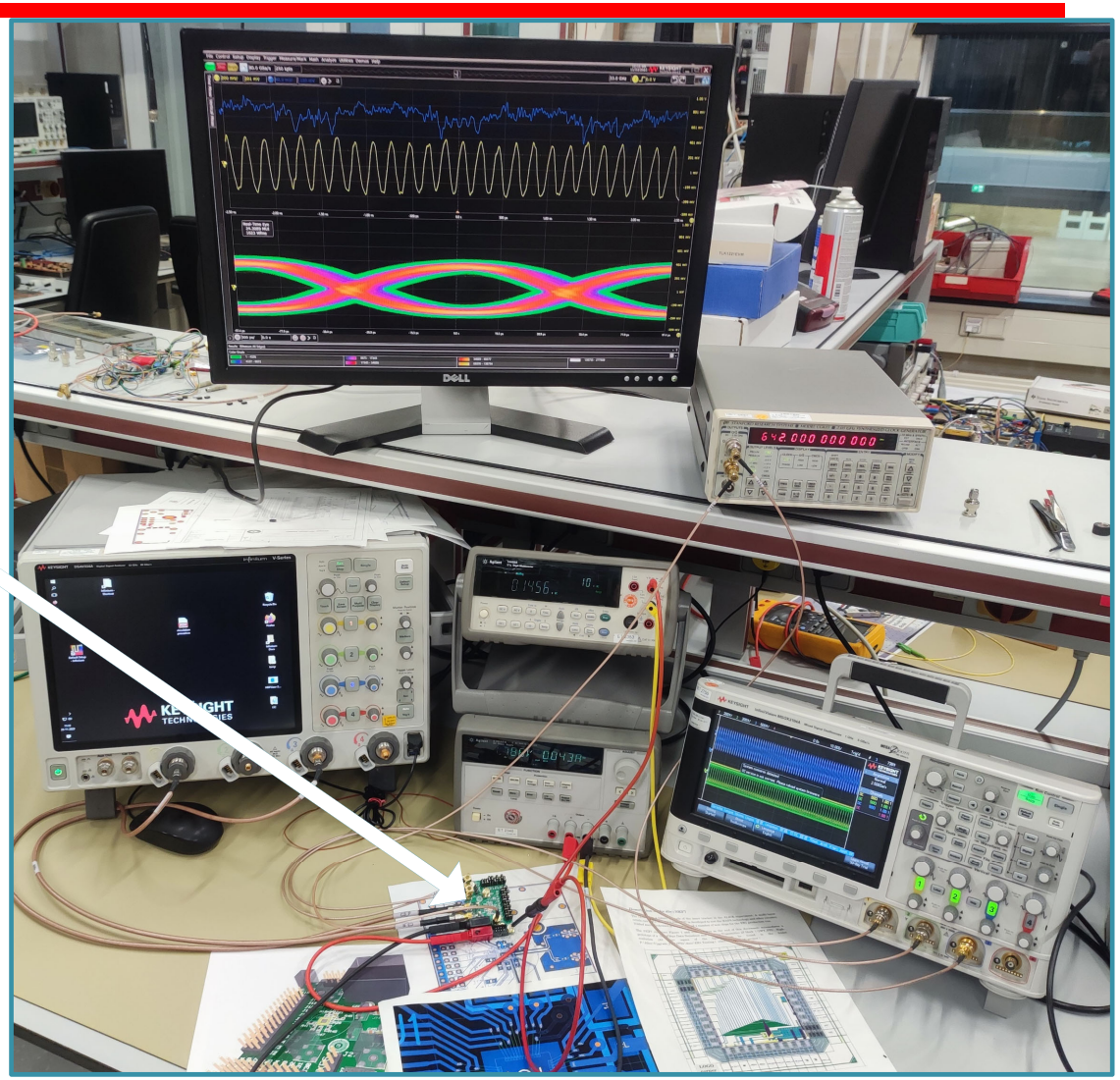


- there will be 6 GWT-PSI blocks integrated in the monolithic stitched sensor chip (MOSAIX)

Validation of the Serializer test chip (NKF7) : experimental setup

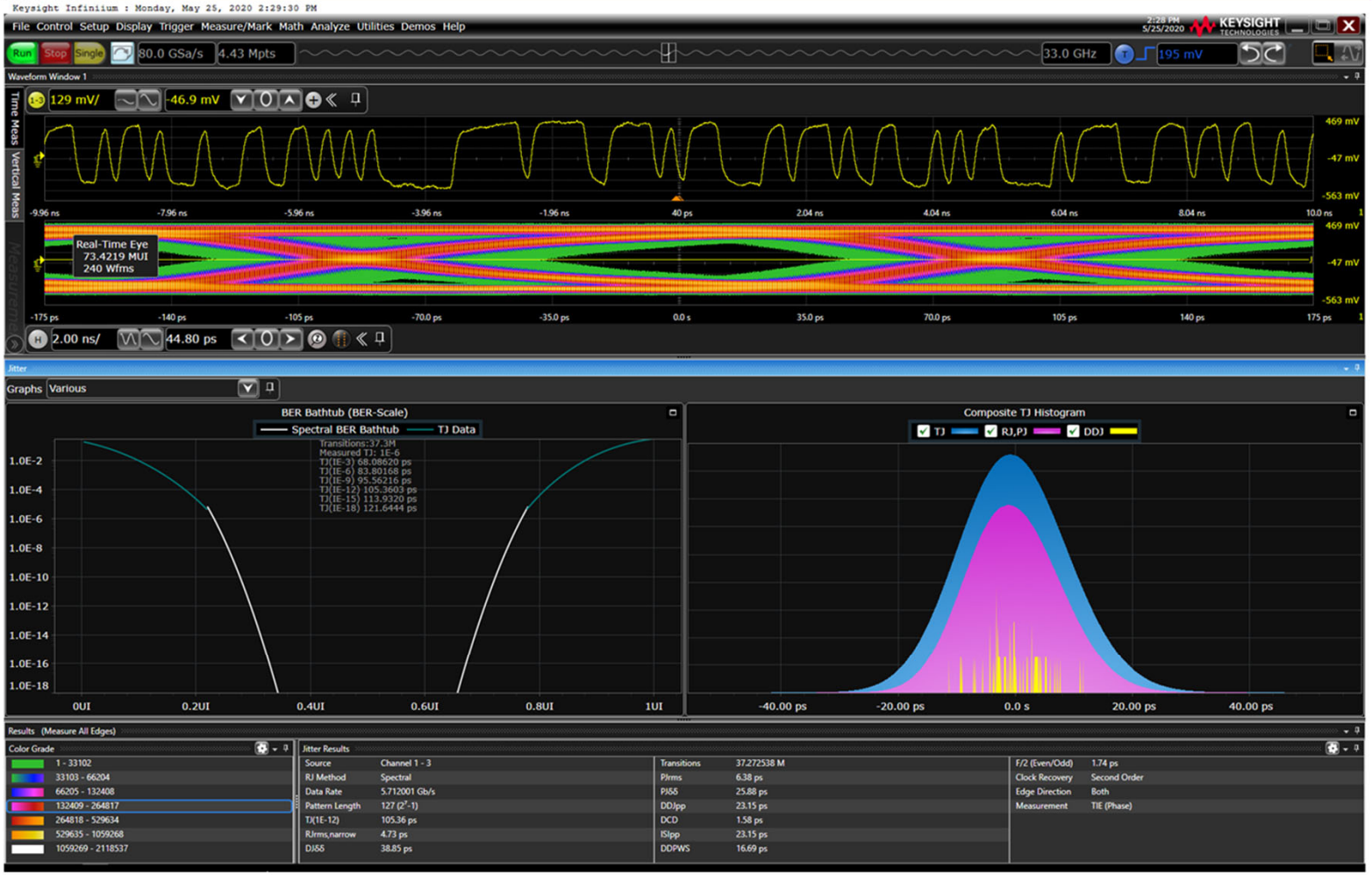
Chip wire-bonded on the pcb





Spare slides

GWT-CC: Bathtub curves and jitter histogram



- the scope locks on the PRBS7 orbit
- the shape of the jitter spectrum looks fine
- the sampling clock tolerance @ BER=10^{-12} is ±0.2UI = ±35ps