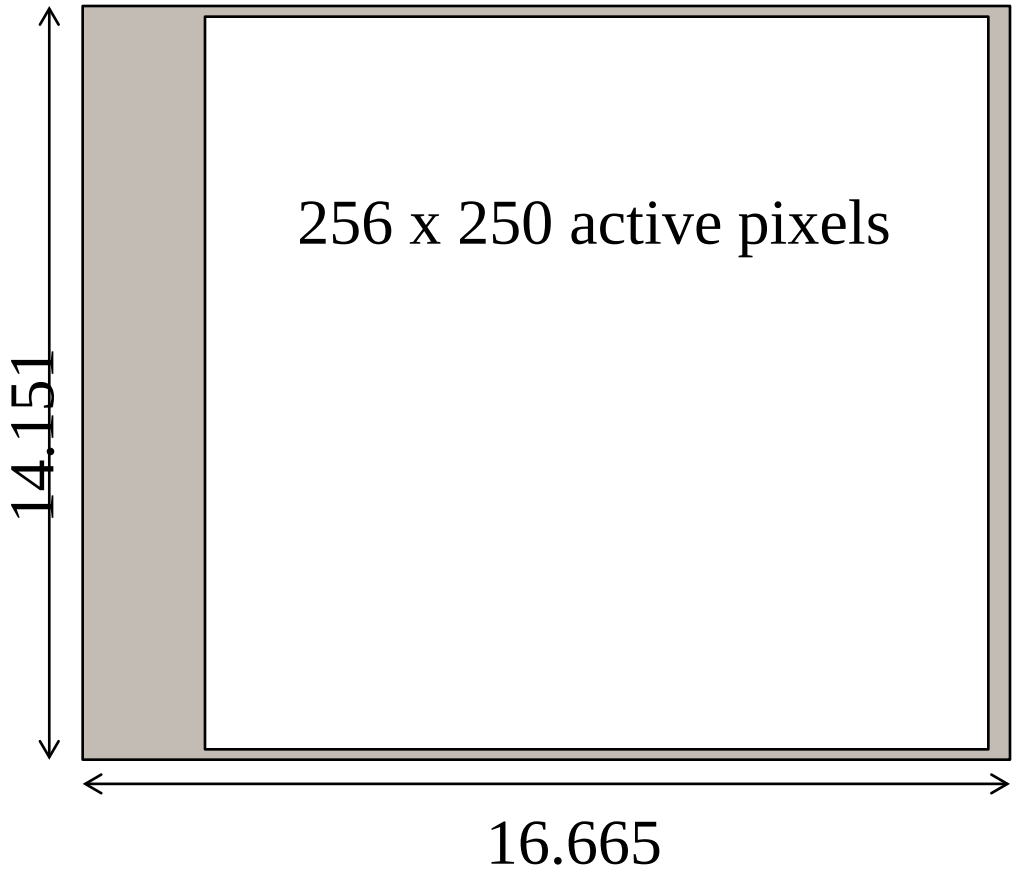
Proposal for a modified InGrid on TPX3

Fred Hartjes
NIKHEF

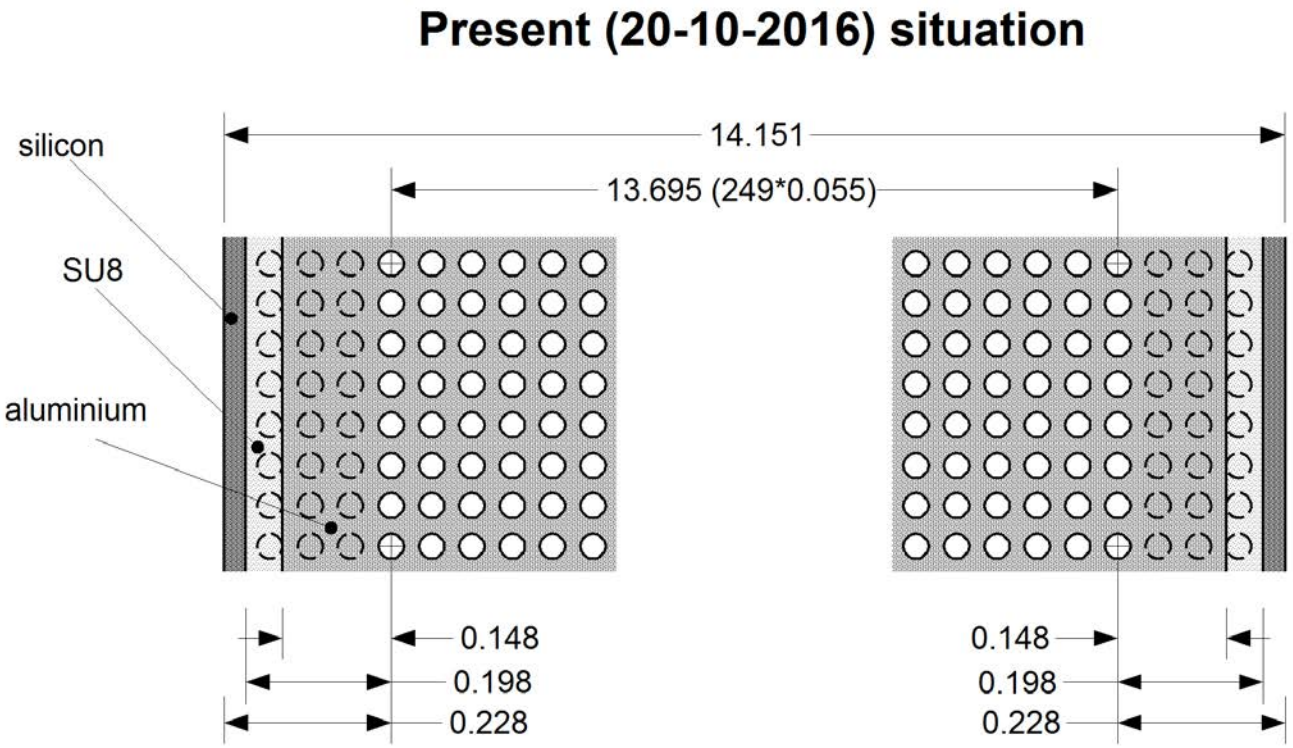
Nikhef/Bonn LepCol meeting
October 24, 2016

Present chip dimensions

- Microscope measurement wit accurate XY stage
- Active fraction of chip surface: 82.1%



Width direction



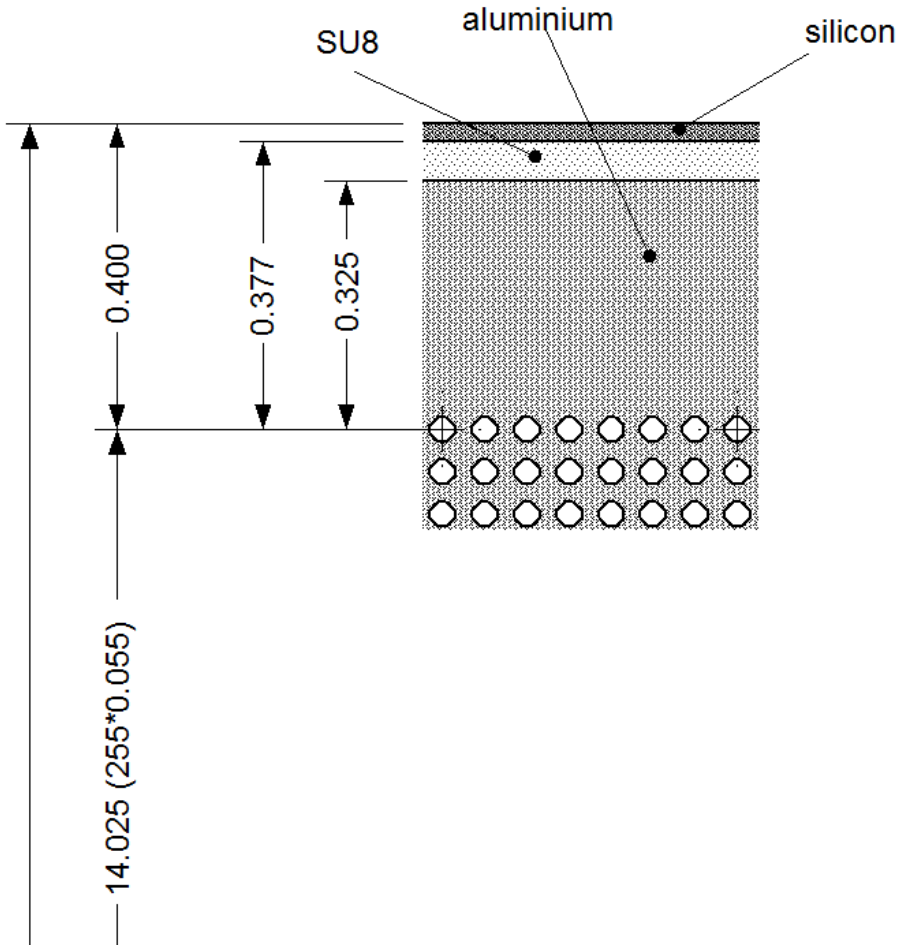
- On left and right side 3 pixel rows are obscured
- Dyke width ~200 µm
- No need to change

Chip top (opposite wire bonds)

Present (21-10-2016) grid design

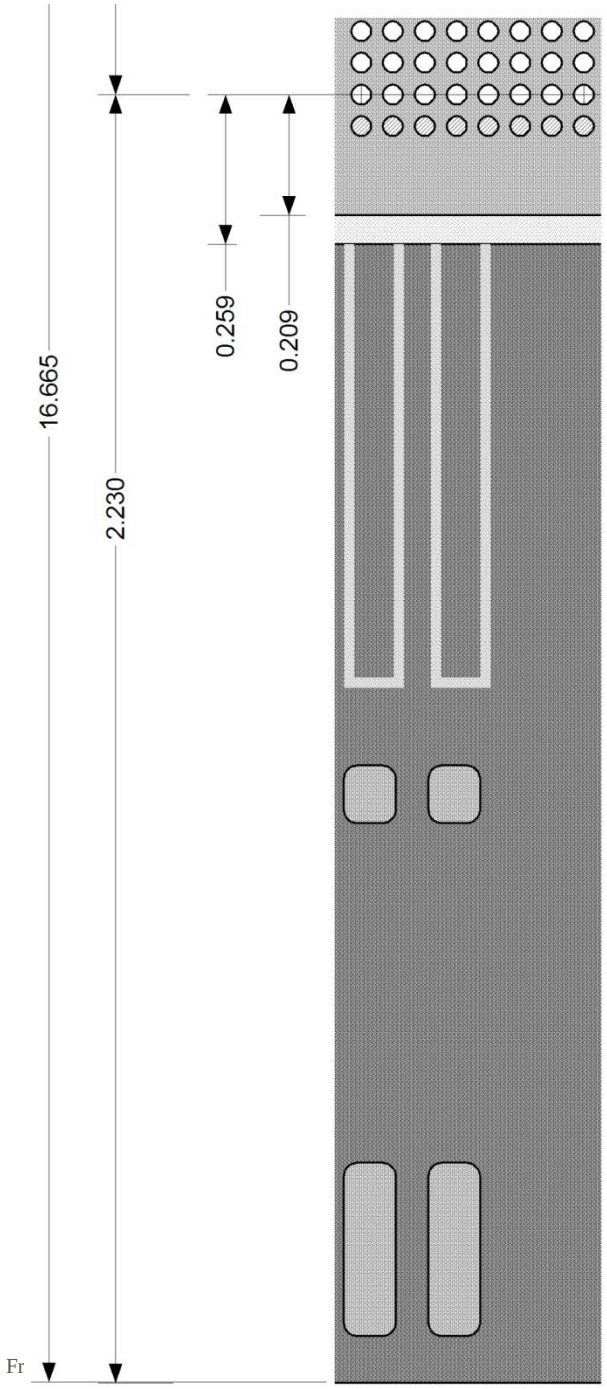
- Dyke quite wide: 377 µm
- But no pixels obscured

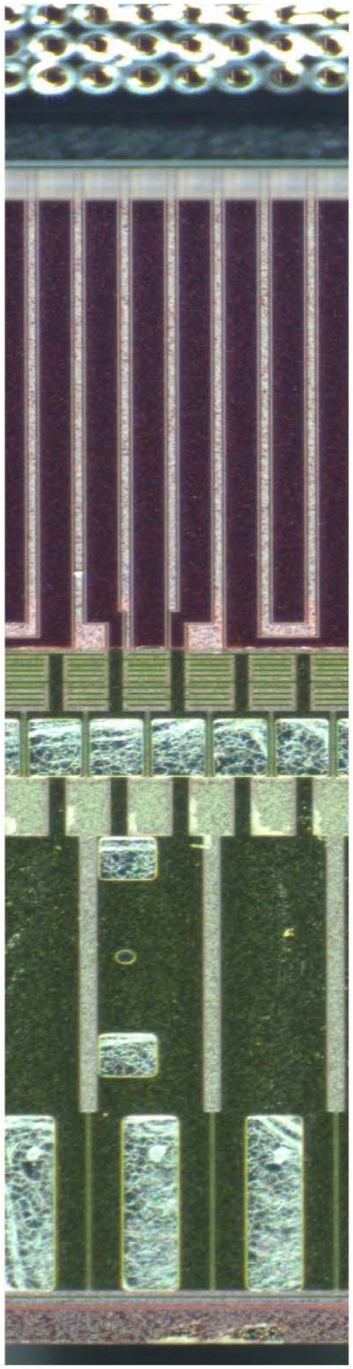
- In fact the chip is a bit (150-200 µm) too long
- It may be hard to reduce the chip height
  - Ruled by interchip distance on the wafer and saw blade width



Wire bond side

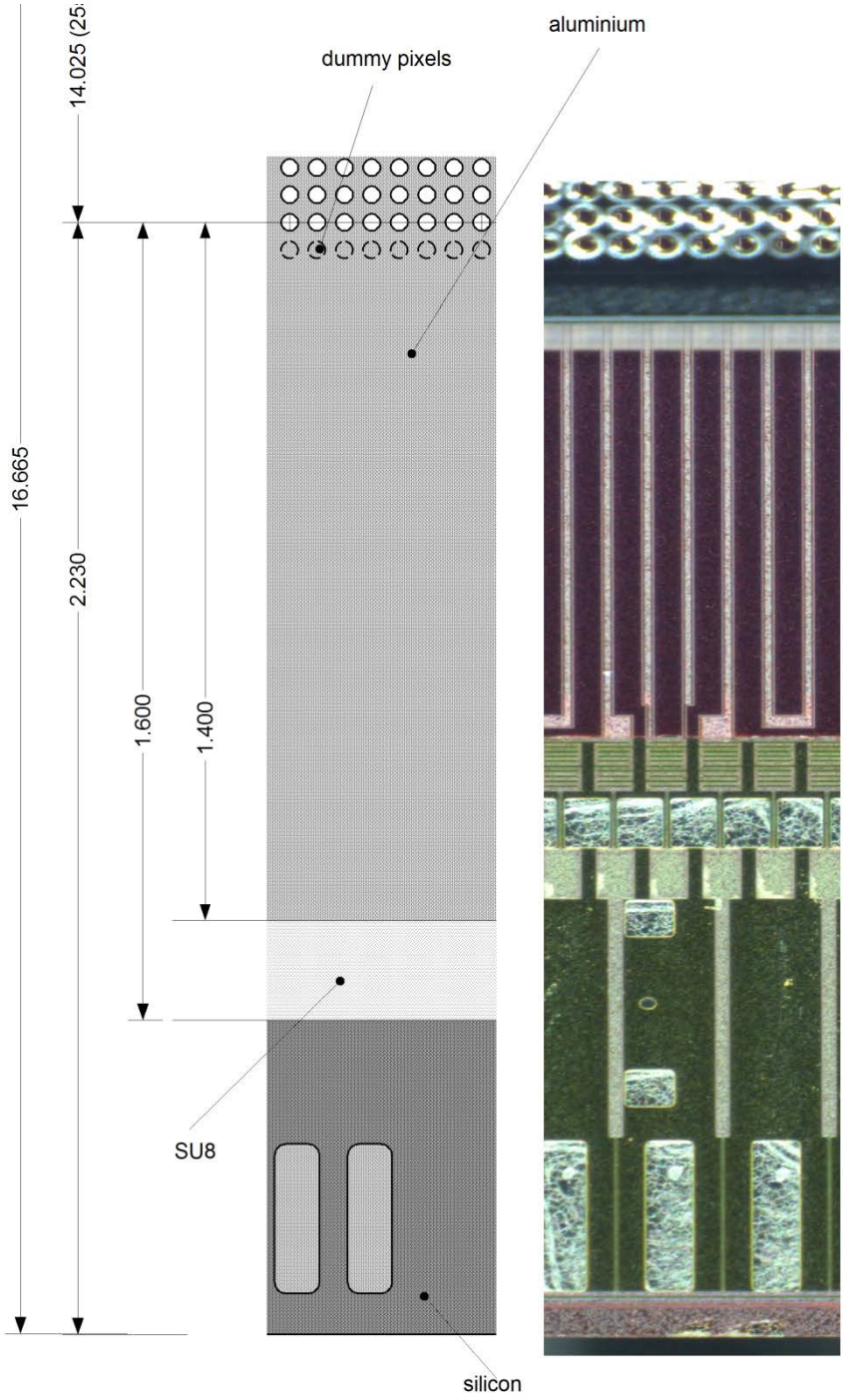
- There are **257** rows of holes in the grid
  - 1st row above dummy pixels
- Width dyke quite narrow: 204 µm to first hole row
  - 50 µm insulation path over SU8
- But we need a wider dyke here
  - Making the HV connection
  - For HV safety we need more insulation path to the wire bonds and chip electronics
- We can easily enlarge the dyke





New proposal wire bond side

- Omit the 257th row of holes above the dummy pixels
- Broaden the dyke from 204 to 1600 µm
  - From 1st active hole row on
- Broaden the grid from 154 to 1400 µm
  - Leaving sufficient space to support the guard electrode
  - Insulation across the SU8 enlarged from 50 to 200 µm



SPARE

List of parameters

- In progress/ under discussion
- Going from one chip to another on same carrier
  - 3 pixels sacrificed
- Going from one chip to another on neighbouring carrier
  - 4 pixels sacrificed
  - 28.6 => 28.435

First approach, to be updated
Put this on a Nikhef server with read access to everybody (incl Bonn)

Mechanical									
Item	**Values (um)**			**Angle (mrad)**		**Reference**			**remarks**
	X	**Y**	**Z**	**hor. Plane**	**vert. plan**	**X**	**Y**	**Z**	
position InGrid of chips	± 20	± 20	± 20	1	1	PCB ref marks	PCB ref marks	foot T	
chip to chip distance	60								
last pixel Ch1 1st pixel CH2	165								
chip to chip distance mod 1 to mod 2	115								
last pixel mod1 to 1st pixel mod 2	220								
module to module pitch	28435								
position PCB ref marks	± 20	± 20	± 100	1	1	carrier edge	carrier edge	carrier foot	
Top guard electrode	± 50	± 50	500± 20	10	1	carrier edge	carrier edge	chip dyke	
chip edge to PBC		100							
chip dimension edge to edge		14130							
Electrical	**Value**								
Grid potential Vgrid (V)	~-400± 4								
Grid supply resistor (Ω)	100M								each chip
drift field E (V/cm)	-100								
Guard potential (V)	Vgrid + E*Zguard								
Guard supply resistor (Ω)	100M								

Assembly / alignment method

- Mount PCB on carrier
  - Refer to two carrier edges using jig with reference marks
  - AND refer to reference marks on PCB
- Mount chips on carrier
  - 2 chips on one side simultaneously
  - XY: refer to grid hole pattern
    - rough alignment using bonding pads (N x 55 µm)
  - AND refer to reference marks on PCB
  - Z: refer to grid (fixed height of alignment jig)
- Mount guard electrode
  - XY: refer edges to reference marks on PCB (tolerance 100 µm)
  - Provide a 1 mm hole at the PCB reference marks
  - Z: let sides of the guard rest on dykes
    - Guard should fabricated bit hollow
- Module to module
  - XY: refer to PCB reference marks

dykes

- Sides
  - 2 x 3 pixels lost
- Top
  - No pixels lost
- Bottom
  - No pixels lost