Mounting /aligning a Quad for LepCol

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All under discussion

Nikhef/Bonn LepCol meeting
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List of parameters

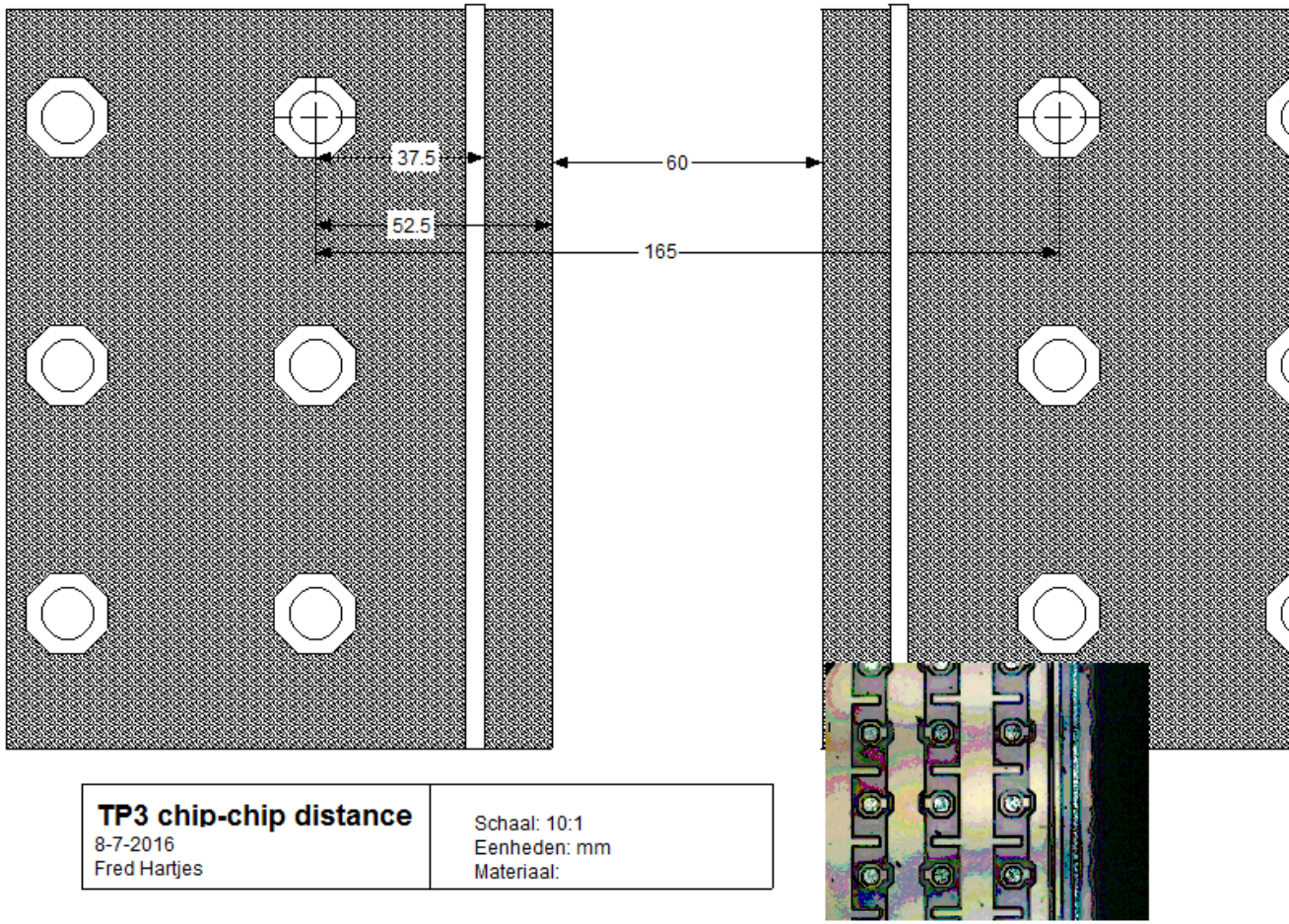
- In progress/ under discussion
- Going from one chip to another on same carrier
  - 3 pixels sacrificed
- Going from one chip to another on neighbouring carrier
  - 4 pixels sacrificed
  - 28.6 => 28.435

First approach, to be updated
Put this on a Nikhef server with read access to everybody (incl Bonn)

Mechanical									
Item	**Values (um)**			**Angle (mrad)**		**Reference**			**remarks**
	X	**Y**	**Z**	**hor. Plane**	**vert. plan**	**X**	**Y**	**Z**	
position InGrid of chips	± 20	± 20	± 20	1	1	PCB ref marks	PCB ref marks	foot T	
chip to chip distance	60								
last pixel Ch1 1st pixel CH2	165								
chip to chip distance mod 1 to mod 2	115								
last pixel mod1 to 1st pixel mod 2	220								
module to module pitch	28435								
position PCB ref marks	± 20	± 20	± 100	1	1	carrier edge	carrier edge	carrier foot	
Top guard electrode	± 50	± 50	500± 20	10	1	carrier edge	carrier edge	chip dyke	
chip edge to PBC		100							
chip dimension edge to edge		14130							
Electrical	**Value**								
Grid potential Vgrid (V)	~-400± 4								
Grid supply resistor (Ω)	100M								each chip
drift field E (V/cm)	-100								
Guard potential (V)	Vgrid + E*Zguard								
Guard supply resistor (Ω)	100M								

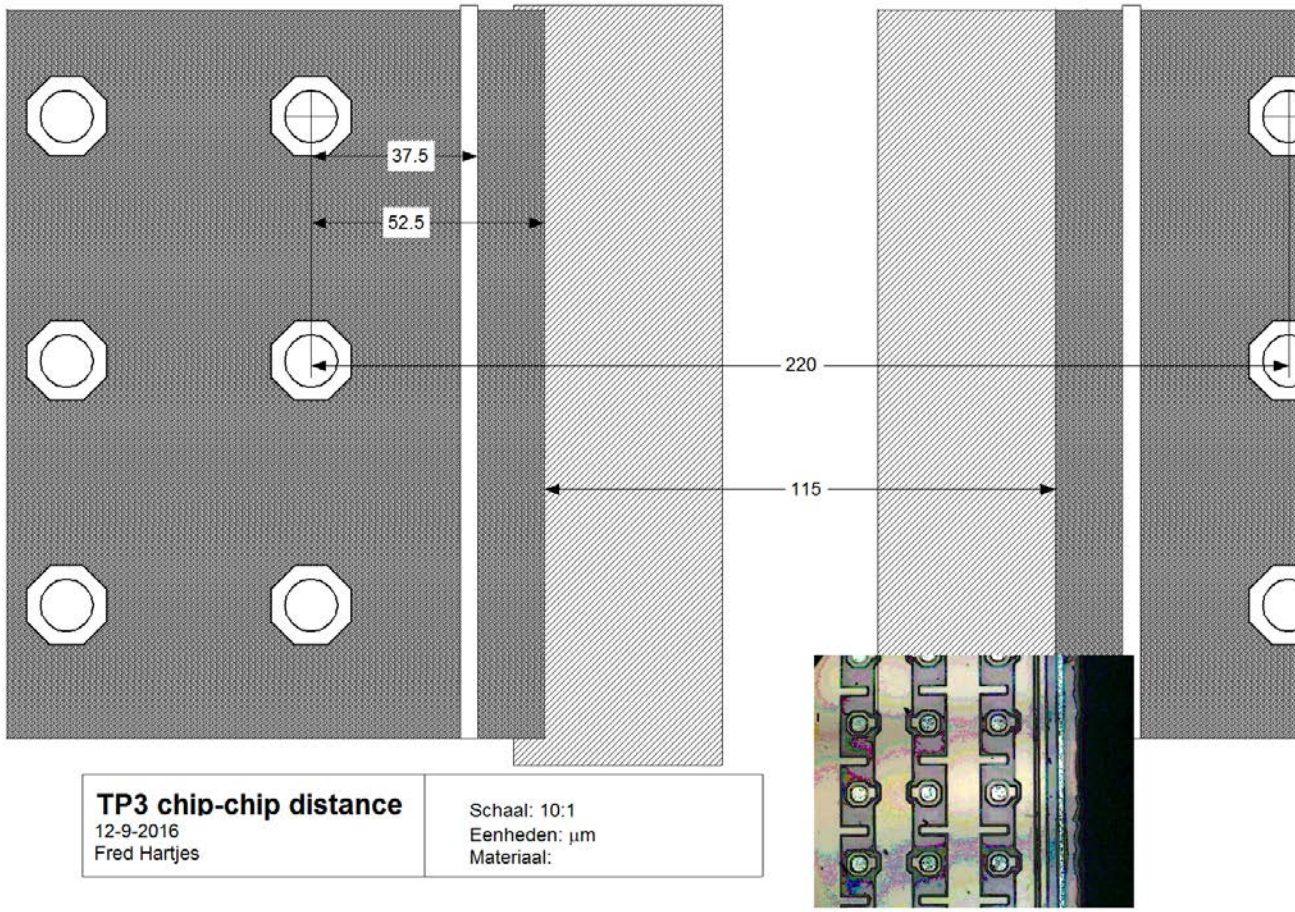
Inter chip distance on same carrier

- Wafer cutting at IZM is very precise
- => We may position the chips very close to another
  - Going from one chip to another only **two** pixels are missing
  - => 165 µm distance between centre last pixel to first pixel
  - 60 µm edge to edge (nominal)
- Info from Martin van Beuzekom



Inter chip distance to another carrier

- Going from one chip to another **three** pixels are sacrified
- => 220 µm distance between centre last pixel to first pixel
- 115 µm edge to edge (nominal)

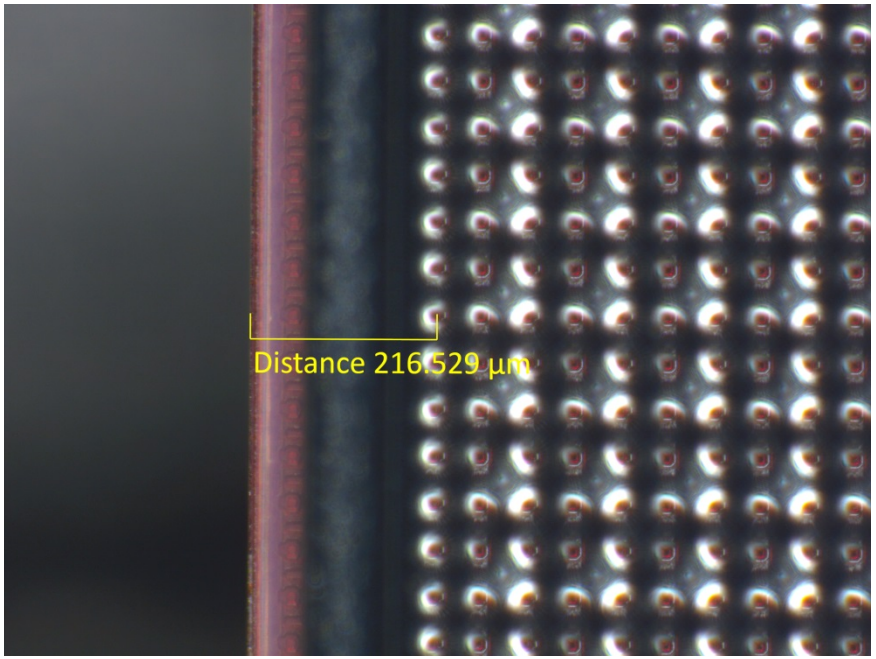


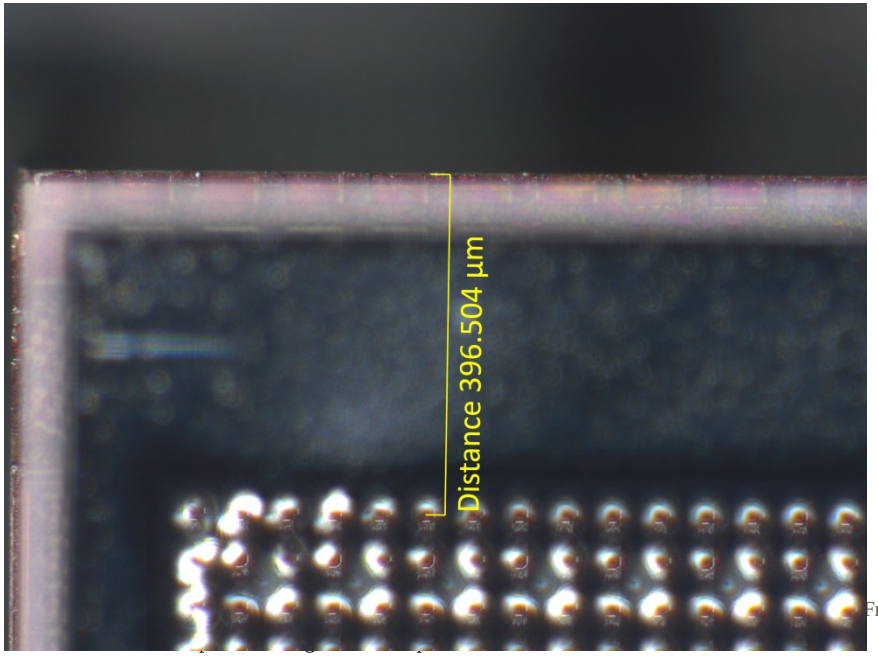
Assembly / alignment method

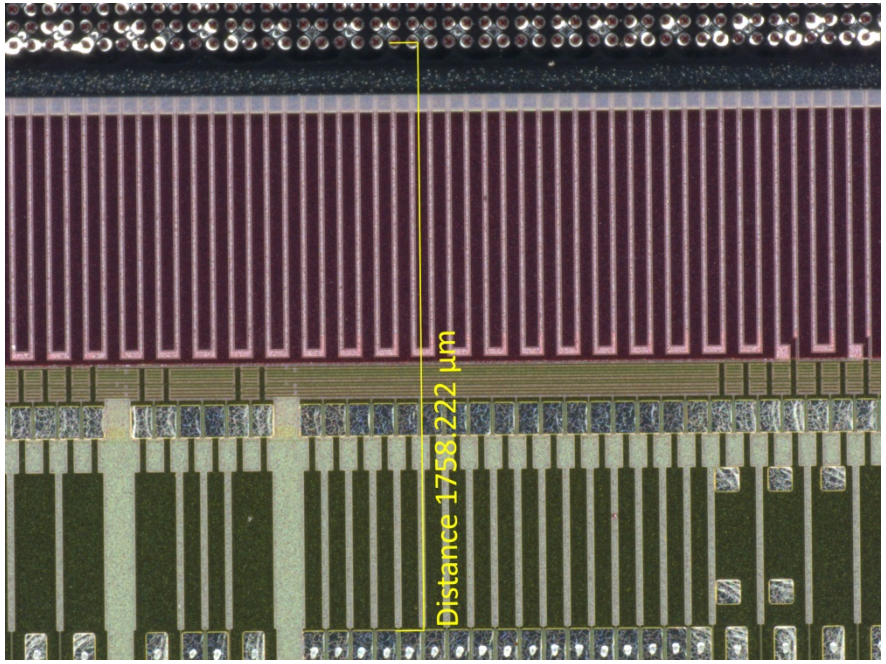
- Mount PCB on carrier
  - Refer to two carrier edges using jig with reference marks
  - AND refer to reference marks on PCB
- Mount chips on carrier
  - 2 chips on one side simultaneously
  - XY: refer to grid hole pattern
    - rough alignment using bonding pads (N x 55 µm)
  - AND refer to reference marks on PCB
  - Z: refer to grid (fixed height of alignment jig)
- Mount guard electrode
  - XY: refer edges to reference marks on PCB (tolerance 100 µm)
  - Provide a 1 mm hole at the PCB reference marks
  - Z: let sides of the guard rest on dykes
    - Guard should fabricated bit hollow
- Module to module
  - XY: refer to PCB reference marks

dykes

- Sides
  - 3 pixels lost
- Top
  - 6 pixels lost
- Bottom
  - No pixels lost







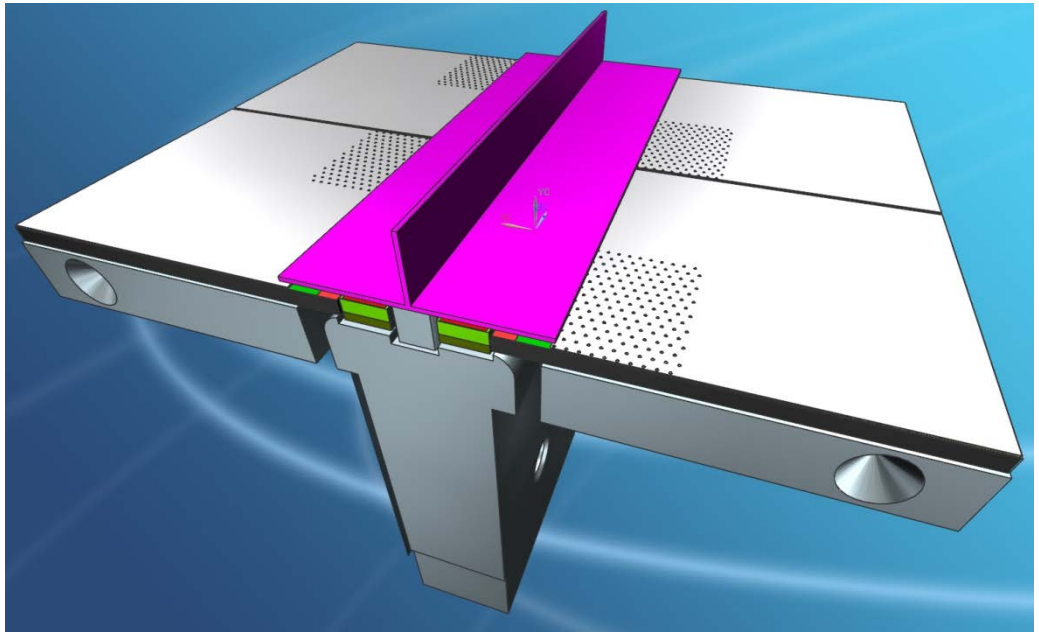
Dyke widths

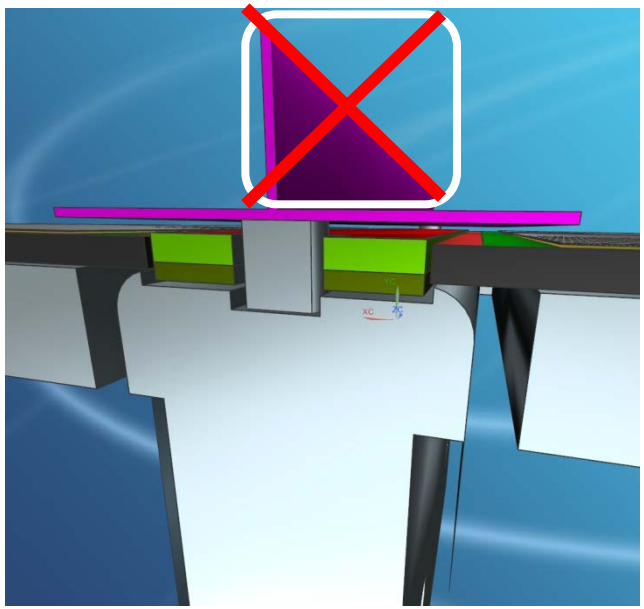
- Presently
  - 256 x 256 = 65536 pixels available
  - 250 x 250 = 62500 (95.4%) used
- Alternative
  - Narrow top dyke to 3 pixels like side dykes
  - => 63250 (96,5%) used
  - Make bottom dyke (wire bond side) very wide ~ 1 mm without obscuring pixels

Reference slides

LepCol Quad type C

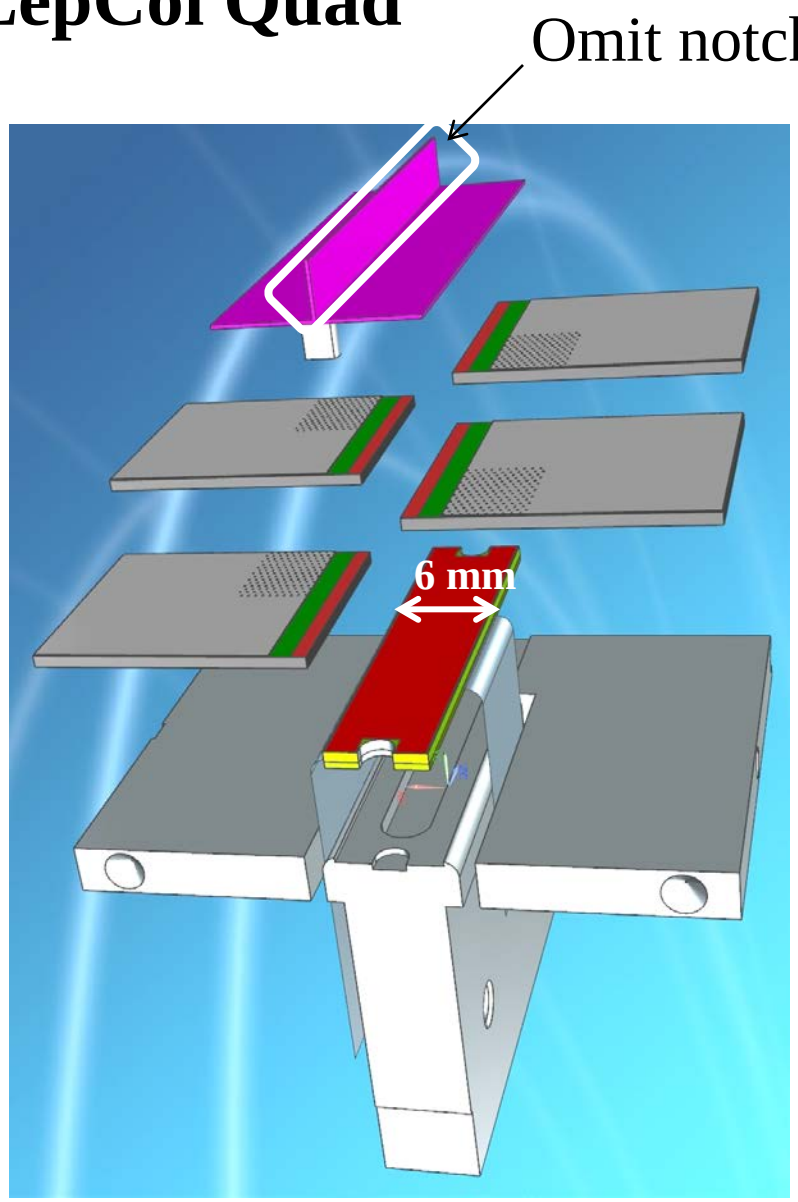
- **Being discussed, design will be adapted**
- **Using 4 TPX3 chips**
  - Glued on carrier
- Grouped around a central PCB for controls, signals and power lines
- Mounted on carrier structure (Aluminium => carbon based material)
- **Active surface ~70%**
- Cooling by common ground plate





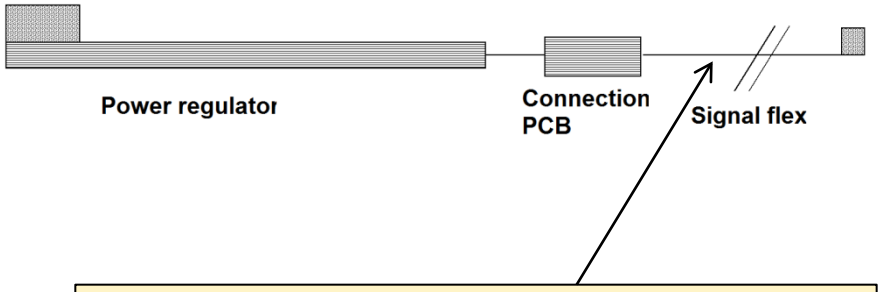
Basic elements of LepCol Quad

1) 4 TPX3 chips + Ingrid
2) Connection PCB
   - **6 mm wide**
   - Flex for
     - Power regulator LV + HV (grid + guard)
     - Signal/ control lines
   - **Flexes loaded from aside**
     - Slits may be very narrow (< 1 mm)
3) Carrier block
   - Initially aluminium
   - To be fabricated in house or by spark erosion
   - Final carbon based material
     - Low mass
     - High thermal conductivity
4) Guard electrode
   - Thin ceramic metalized plate
   - Third support point will be added

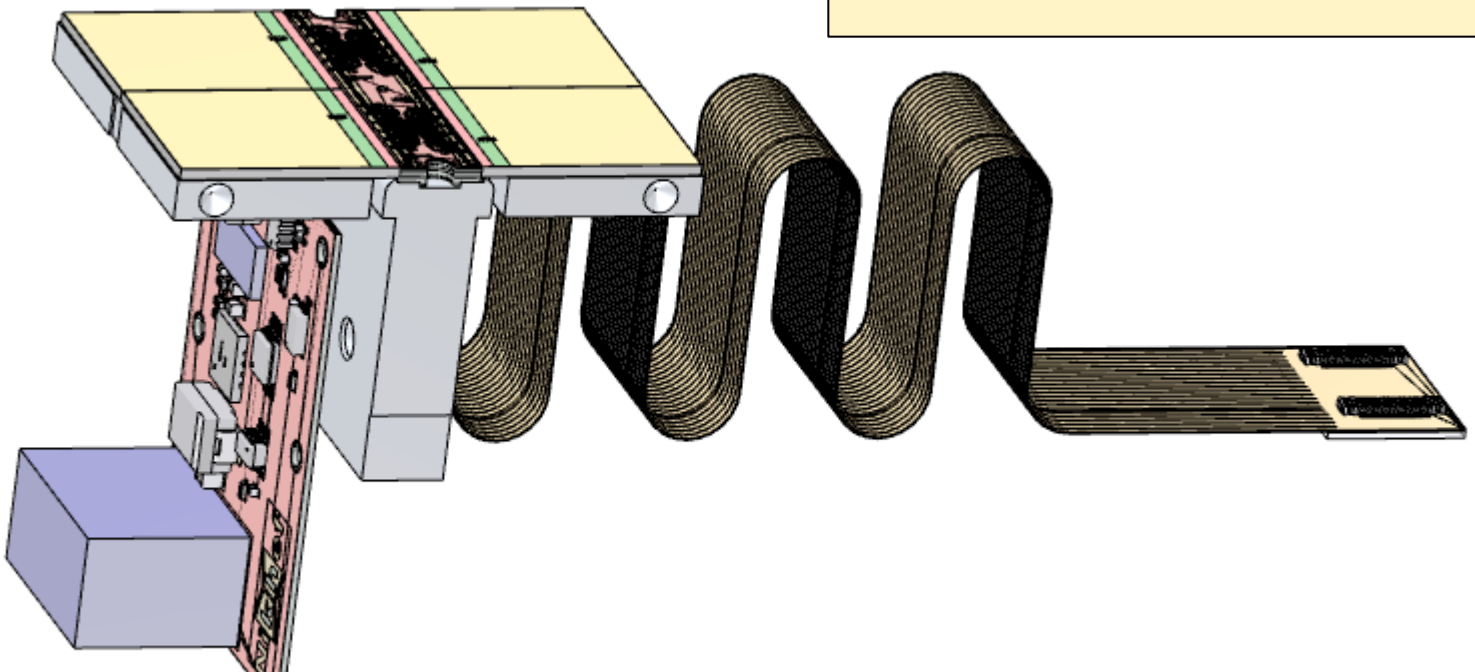


Electronics

- Power regulation close to chips (< 2 cm)
  - Stabilising supply voltage from ~2.5 to 1.5 V
- Central PCB + signal flex + power board in one piece
  - No connectors between these elements
- ~20 W on power has to be cooled via carrier block
  - Max 40 W for extreme occupancy

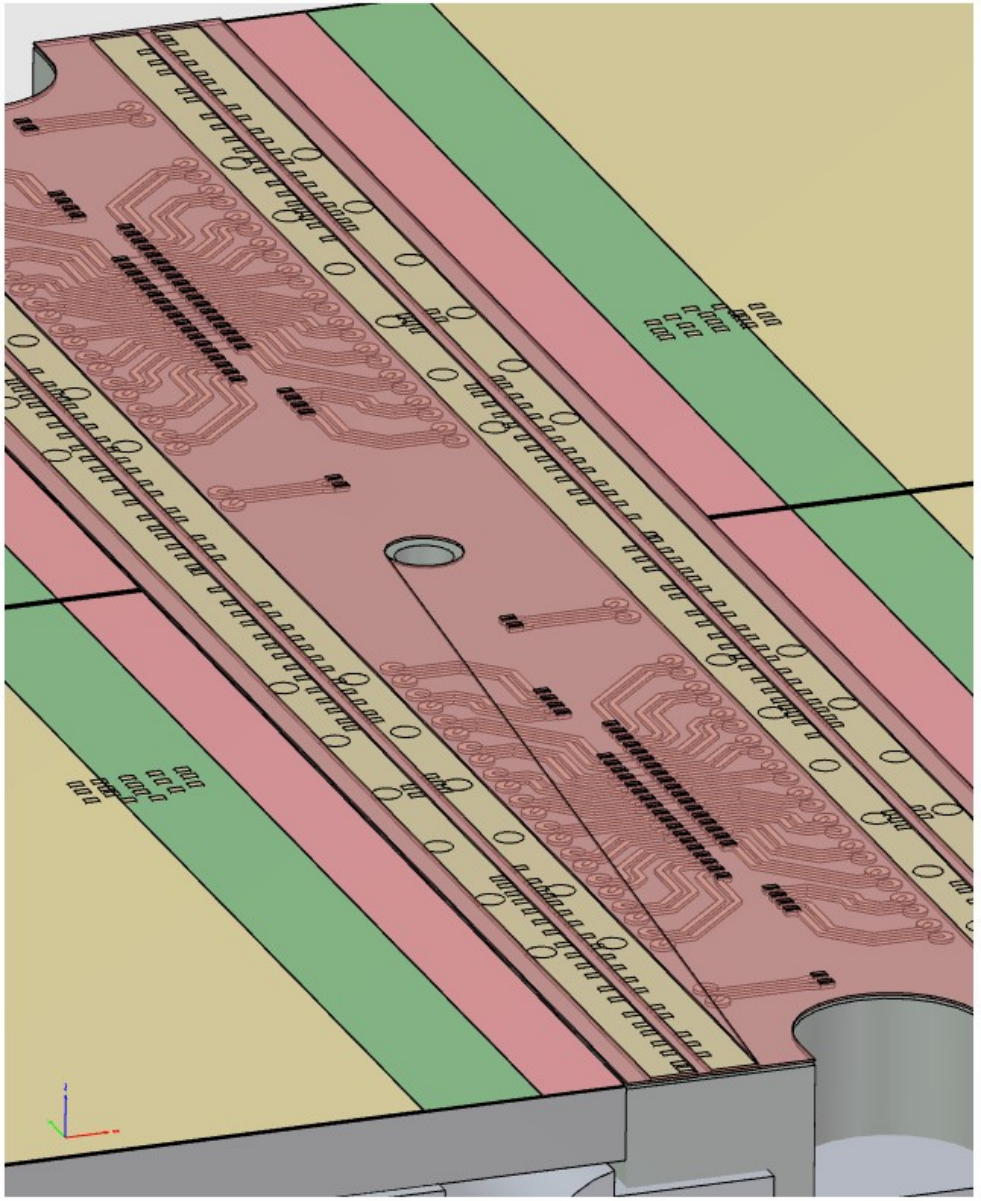


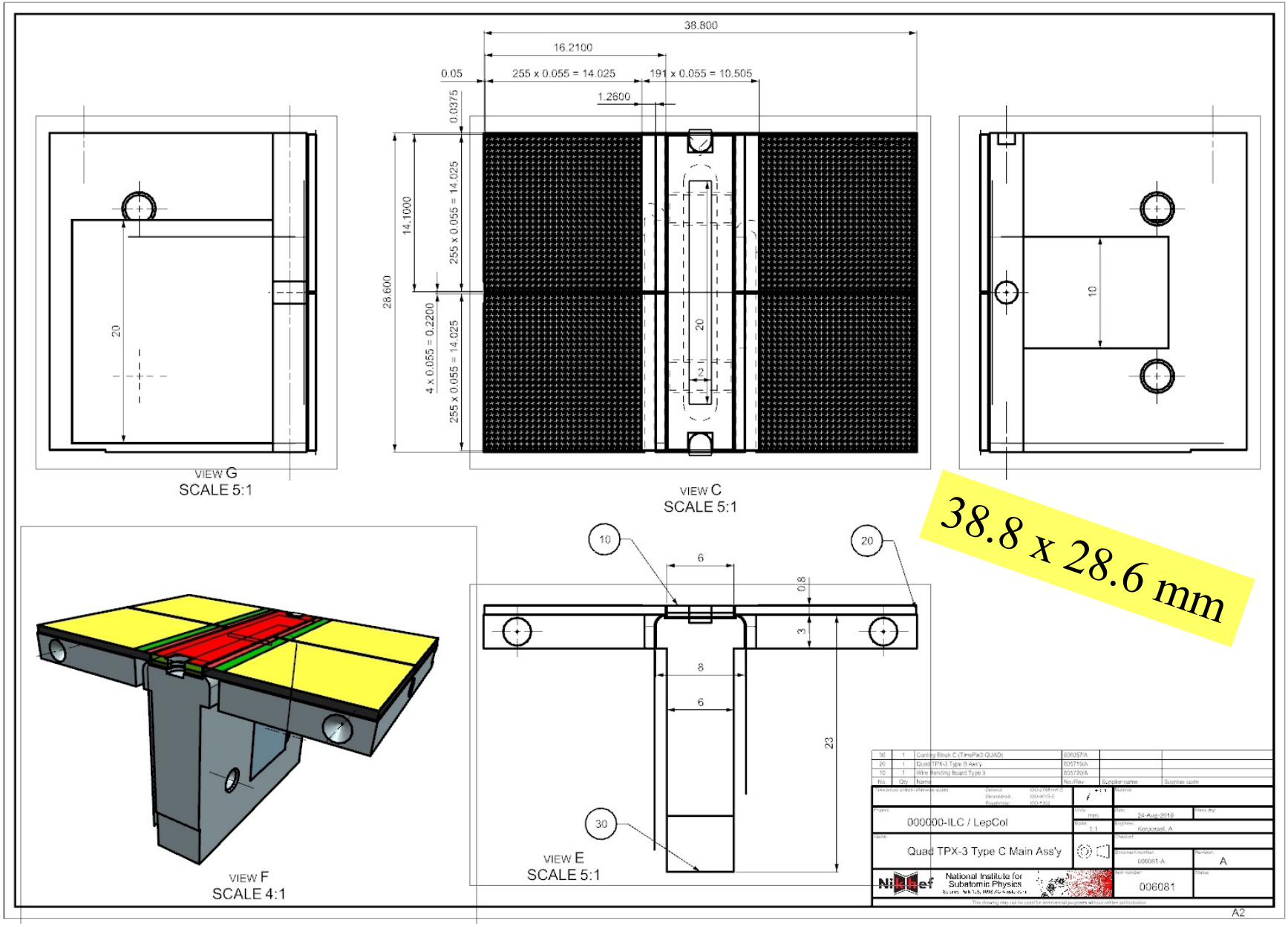
Flex with control and output signals may be long (up to 20 cm)



PCB with traces

- 19 metal layers
- Additional hole in centre for guard support




38.800
16.2100
0.05
255 x 0.055 = 14.025
191 x 0.055 = 10.505
1.2600
0.0375
14.1000
255 x 0.055 = 14.025
28.600
4 x 0.055 = 0.2200
255 x 0.055 = 14.025
20
10
VIEW G
SCALE 5:1
VIEW C
SCALE 5:1
38.8 x 28.6 mm
VIEW F
SCALE 4:1
VIEW E
SCALE 5:1
000000-ILC / LepCol
Quad TPX-3 Type C Main Ass'y
National Institute for Subatomic Physics
006081
A2