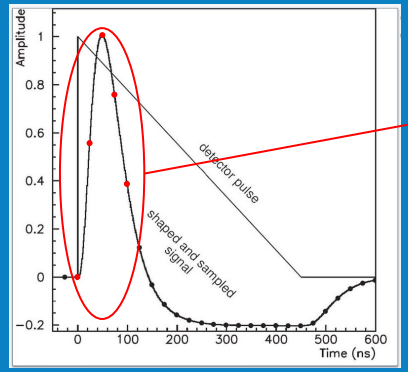
Embedded Neural Networks on FPGAs for Real-Time Computation of the Energy Deposited in the ATLAS Liquid Argon Calorimeter

Raphaël BERTRAND

Aix Marseille Univ, CNRS/IN2P3, CPPM, Marseille, France

Introduction



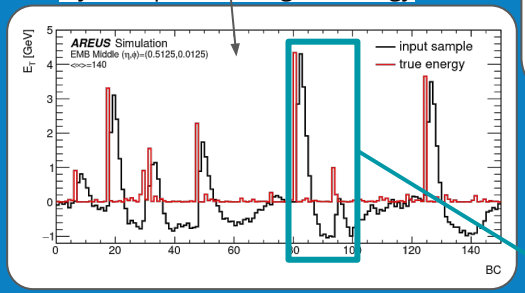
$$E_t = \sum_{i=1}^{5} c_i * x_{t+i}$$

Simulated pulse chain with additional injected pulses at higher energy

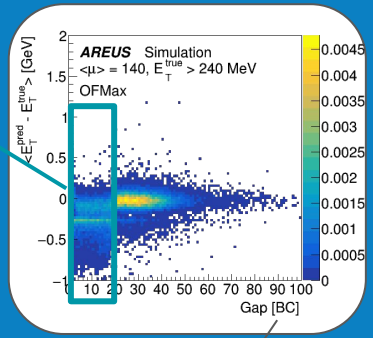
Energy deposits in LAr calorimeter cell→electric pulse

- **shaped**
- **sampled**
- **digitized** at **40 MHz**

The pulse **spans** about **625 ns**.



Region where pulses overlap



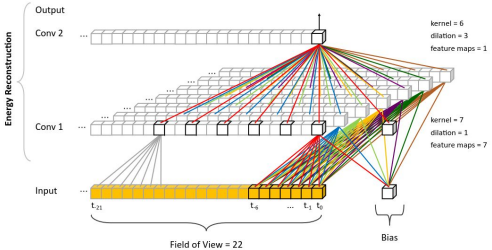
Bunch Crossing : 25 ns

- HL-LHC **high pileup → OF performance degradation**
- Neural networks are investigated as an alternative solution to the OF algorithm.

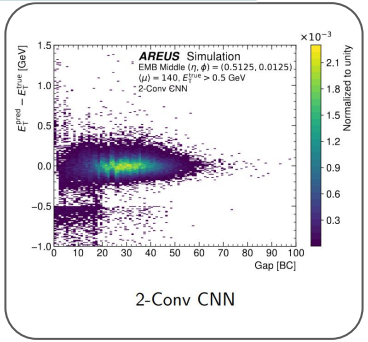
Neural network structure

CNN with ~100 parameters

Energy prediction for every BC

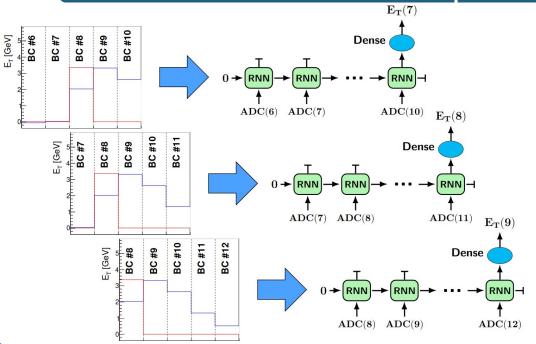


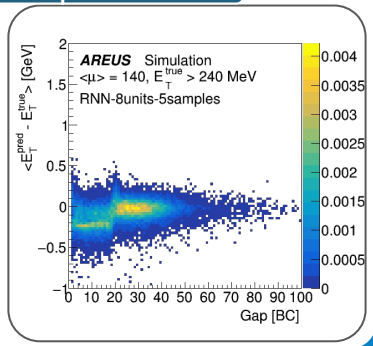
Continuous input from one detector cell



2-Conv CNN

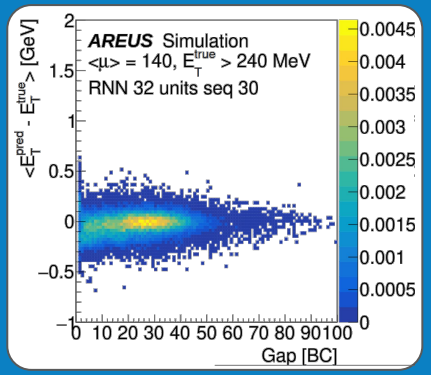
RNN 8 units 5 input samples





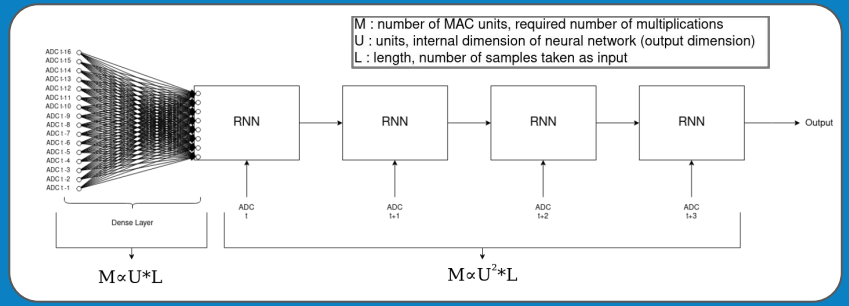
- **CNNs** and **RNNs** are designed to **compute deposited energy**.
- **NNs can correct the degradation** of the energy resolution.

Optimization of the RNN



RNN with 8 units and 5 samples as input can be upgraded :

- Increase nb of units
  ↳ better resolution overall
- Increase nb of input samples
  ↳better resolution with overlapped pulses



Increasing the number of units and input samples go with more computations and it can't be implemented.

- Dense Layer as input of the 1st RNN cell for input samples before the energy deposit.
  - RNN cells to compute the amplitude on the peak
  - Dense to correct for the pileup

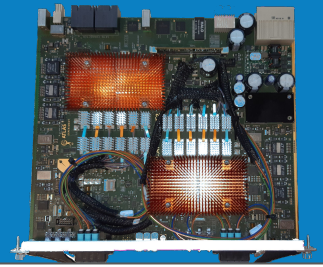
Firmware implementation

LASP demonstrator built with Stratix-10

- prototype with Agilex 7 ongoing

Each FPGA needs to reconstruct the energy for 384 channels :

- Impossible to implement 384 NNs on the FPGA
  - Need multiplexing
  - Need higher frequency



LASP board demonstrator

RNN and CNN Implemented on Stratix-10

- CNN implemented on Agilex, RNN still in progress
- CNN directly implemented in VHDL, RNN Implemented first in HLS for fast prototyping and then optimized in VHDL
- Fits LAr requirements for both

FPGA	Network	Multiplex.	Detector cells	f_{max}	ALMs	DSPs
Stratix-10	RNN (HLS)	10	370	393 MHz	90 %	100 %
	RNN (VHDL)	14	392	561 MHz	18 %	66 %
	CNN (100 param.)	12	396	415 MHz	8 %	28 %
Agilex	CNN (100 param.)	12	396	539 MHz	4 %	13 %
	CNN (400 param.)	12	396	510 MHz	19 %	50 %