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Deep Learning-Based Data Processing in Large-Sized Telescopes of the Cherenkov Telescope Array: FPGA Implementation and Performance Comparison with GPUs

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The Large-Sized Telescope (LST) is one of three telescope types being built as part of the Cherenkov Telescope Array Observatory (CTAO) to cover the lower energy range between 20 GeV and 200 GeV. The Large-Sized Telescope prototype (LST-1), installed at the La Palma Observatory Roque de Los Muchachos, is currently being commissioned and has successfully taken data since November 2019. The construction of three more LSTs at La Palma is underway. A next generation camera that can be used in future LSTs is being designed. One of the main challenges for the advanced camera is the 1GHz sampling rate baseline that produces 72 Tbps of data. After filtering events resulting from random coincidences of background light sources (night sky background, star light, sensor noise), the data rate must be brought down to 24 Gbps, corresponding to an event rate of about 30 kHz. At this stage, a software stereo trigger featuring deep learning inference running on a high-speed FPGA will lower the final event rate to < 10 kHz.

To achieve such a large reduction, several trigger levels are being designed and will be implemented in FPGA. The final trigger stage is a real-time deep learning algorithm currently under development. In this talk, we will focus on porting this algorithm to FPGAs using two different approaches: the Intel AI Suite and the hls4ml packages. Then we compare the performance obtained in FPGAs against running it in GPUs.

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