Concept of a LepCol module with TimePix 3

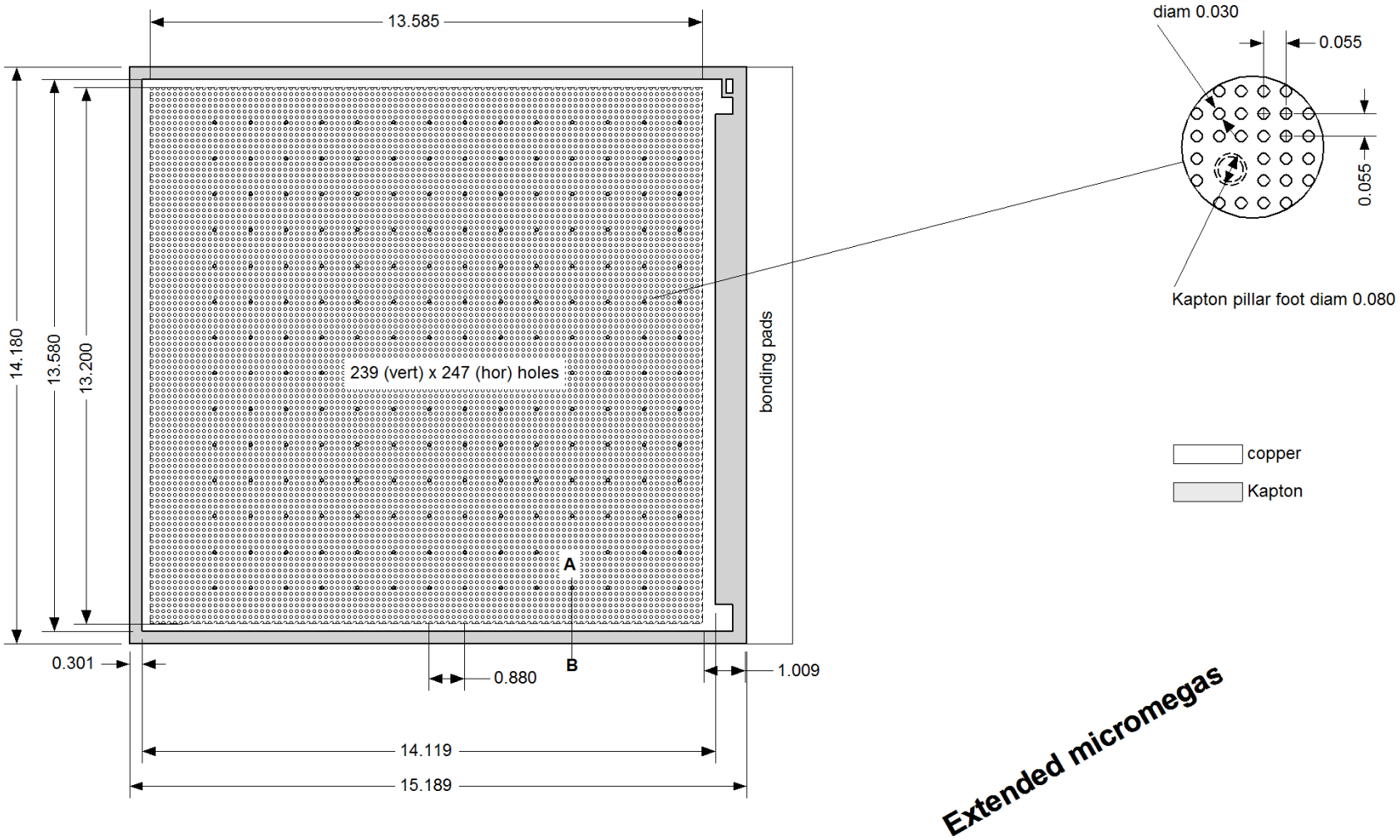
Very first stage of development

Ideas of Harry and Fred,
Charles Ietswaard and Bas van der Heijden,
Auke Korporaal
NIKHEF

LepCol meeting Nikhef
June 6, 2016

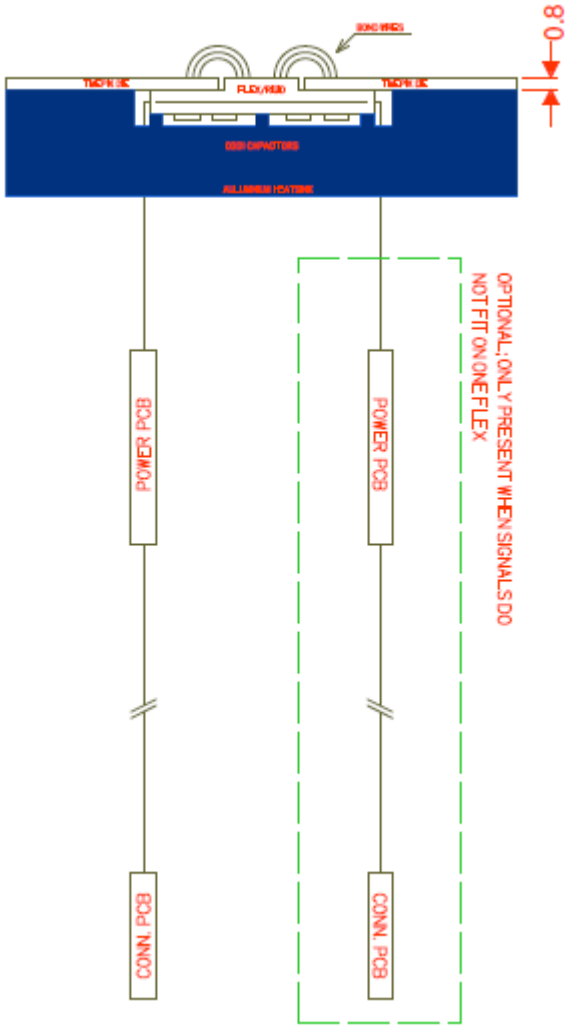
Micromegas on TimePix 3 chip

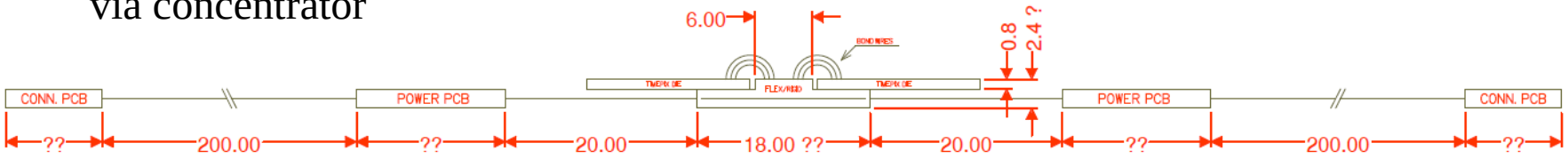
- Present module design based on future extended Micromegas approach
  - Actual design has 1 mm shorter grid
- Yevgen InGrid design may have bit more active area



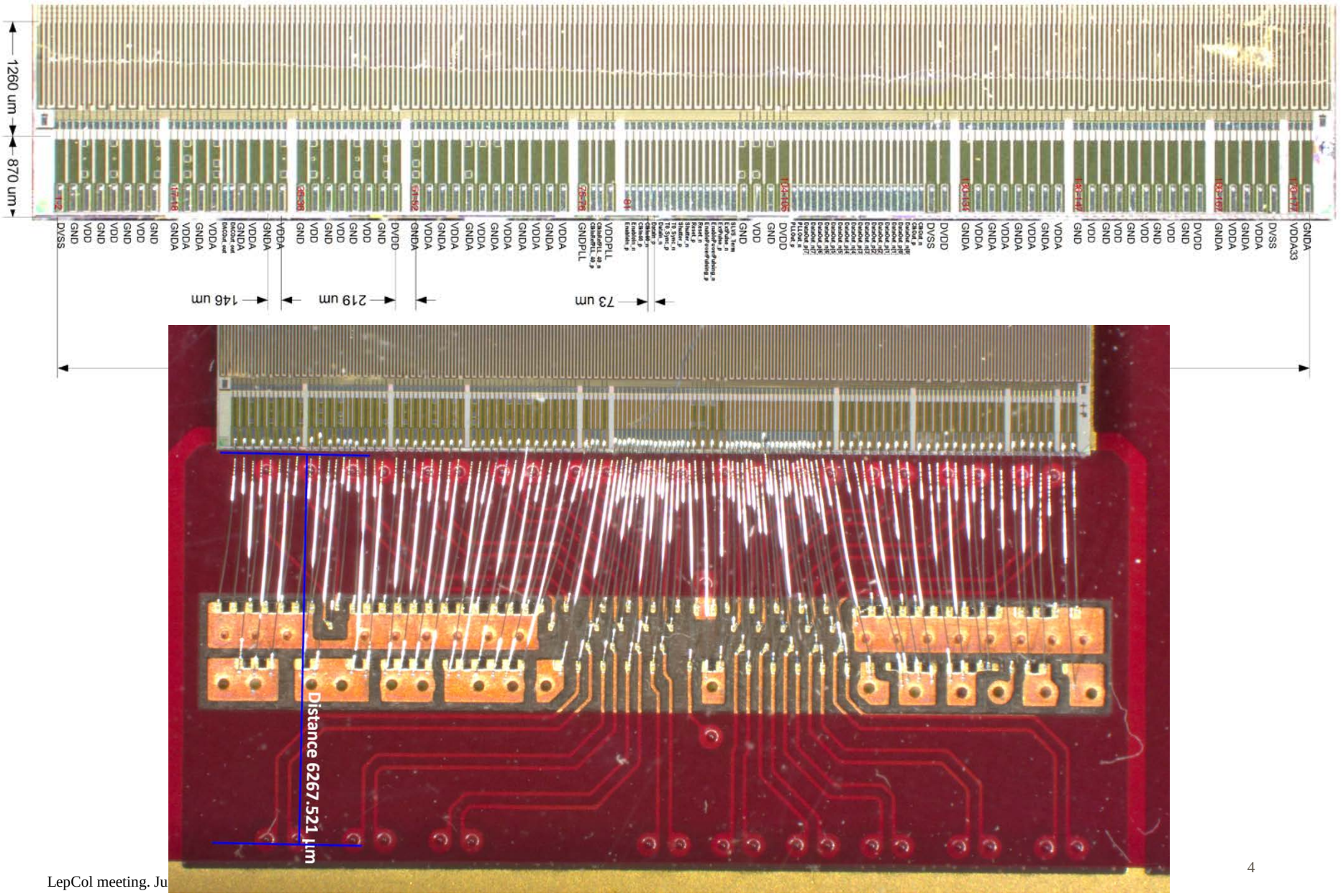
Discussion with Charles and Bas

- **2 chips facing another**
  - **Single chip row costs more space**
- PCB width **6 mm** at chip surface
  - Due to space for wire bonding and traces
- Minimum pad pitch on PCB: 100 um
  - 73 um on TPX3, => fanning in
- We may omit 2 x 7 of the 2 x 8 DataOut lines
  - => max hit rate 1.5 MHz
  - But we cannot omit the 17 control lines
- Output to two flex pcbs
  - Maybe one will do
- Voltage regulator close to bonding pads (≤ 2 cm)
  - 2 V => 1.5 V
- DC-DC converter (anti magnetic)
  - 35 V => 2 V
- Connection of many modules to FPGA board (Xylinx) via concentrator



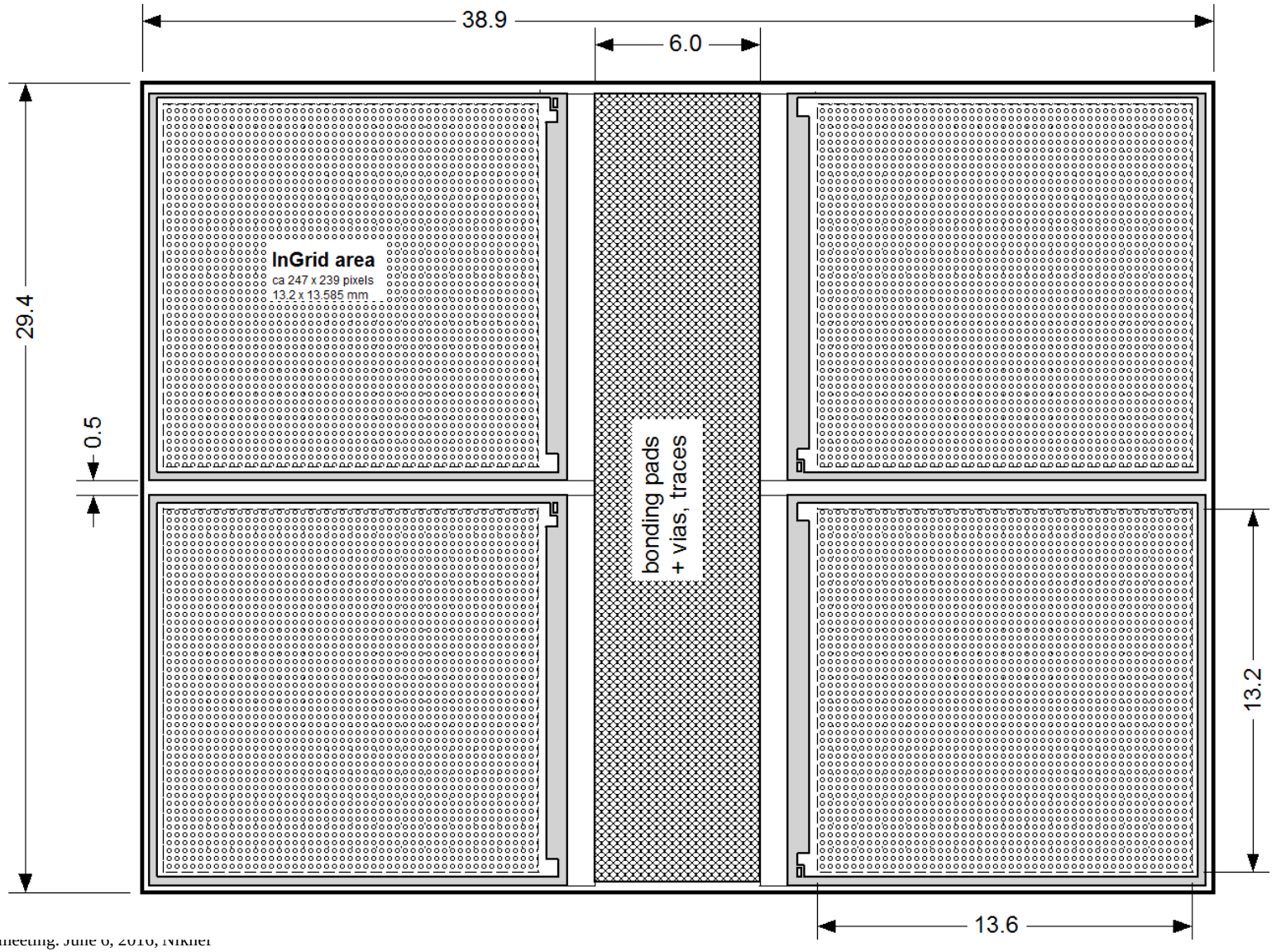


Bonding the TimePix-3



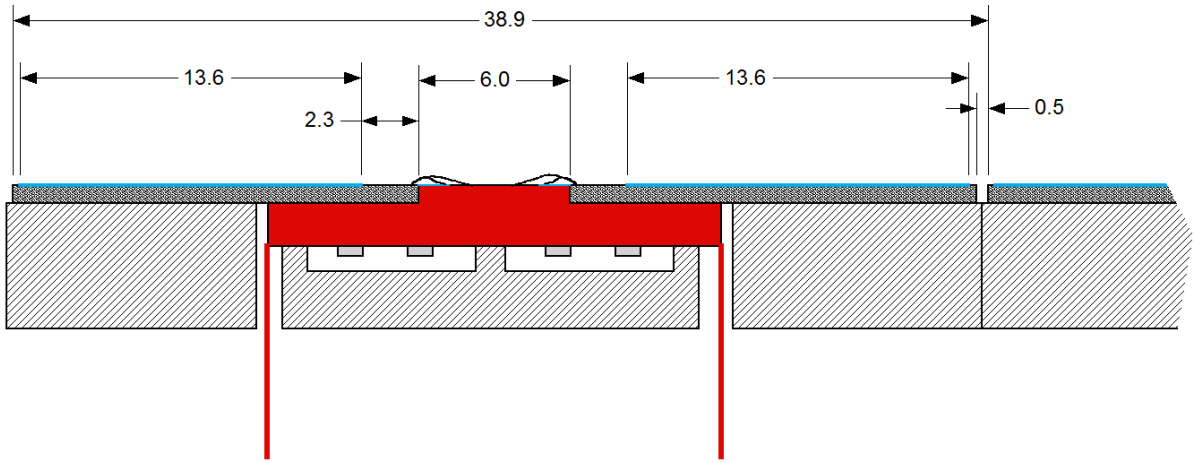
GridPix building block

- Adding more chips to the module is possible, but has probably no advantage



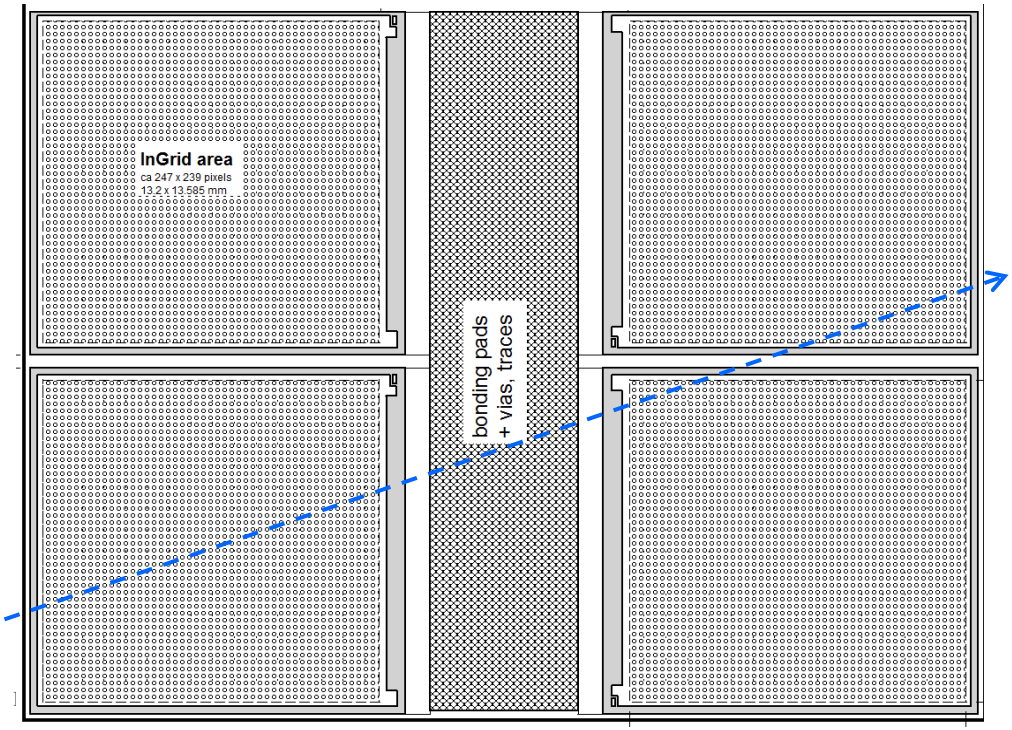
Active area

- 6 mm distance between chips at bonding pad side
- 0.5 mm spacing at other sides
- Cooling by cold plate under the module
  - CO2 or water



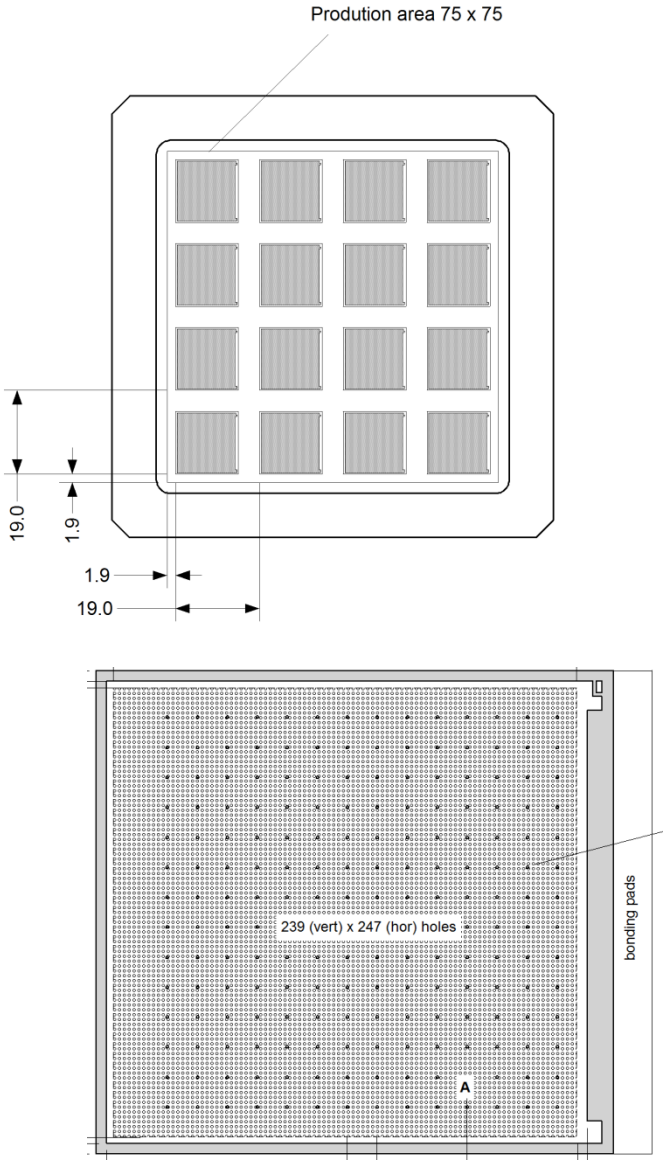
- Module surface
  - **11.44 cm2**
- Module active area
  - **4 x 1.795 = 7.18 cm2**

- **=> Active area 62.8%**



GridPix development on TPX3

- Yevgen at IZM now preparing an InGrid production on a TPX3 wafer
- Nikhef plan B: mounting a dedicated Micromegas foil on a protected TPX3 chip
  - Practical identical to InGrid
  - First foil has arrived (16 micromegas patterns)
  - Specified as mechanical tests only
    - But possibly most micromegas can be used
  - Assembly method in development
- Spark tests at Nikhef going on
  - TPX3 chips (broken) with SiC being produced



Provisional budget for developing a 4-chip LepCol module

Subject	Person	Time (wk)	Cost (k€)
Schematics of the PCB, flex and concentrator board	Bas	16	
Layout + production 1st + 2nd PCB	Charles	3	7 + 5*
Concentrator layout	Charles	2	2
RO board	Bas	1	2
Mechanics design	Auke	9	2
Mechanics production	MT	4	PM
Lab costs			10
TOTAL		**34**	**28**

- Time schedule
  - Depending on the availability of the staff a first prototype could be completed in spring 2017

* 2nd revised PCB is assumed

Summary

- **Start LepCol TPC project with designing a small building block first**
- PCB + RO is ruling the concept
- Generic design, not LepCol specific, may be used for every TPC
- Two rows of chips sharing a single PCB is most surface effective
  - Module may have 4, 6, 8, ……. chips
  - But more than 4 chips has probably no advantage
- Active surface may cover 60 – 65% of module's total surface
- Field shaping not incorporated yet, but solvable

Let's limit ourselves to a modest start