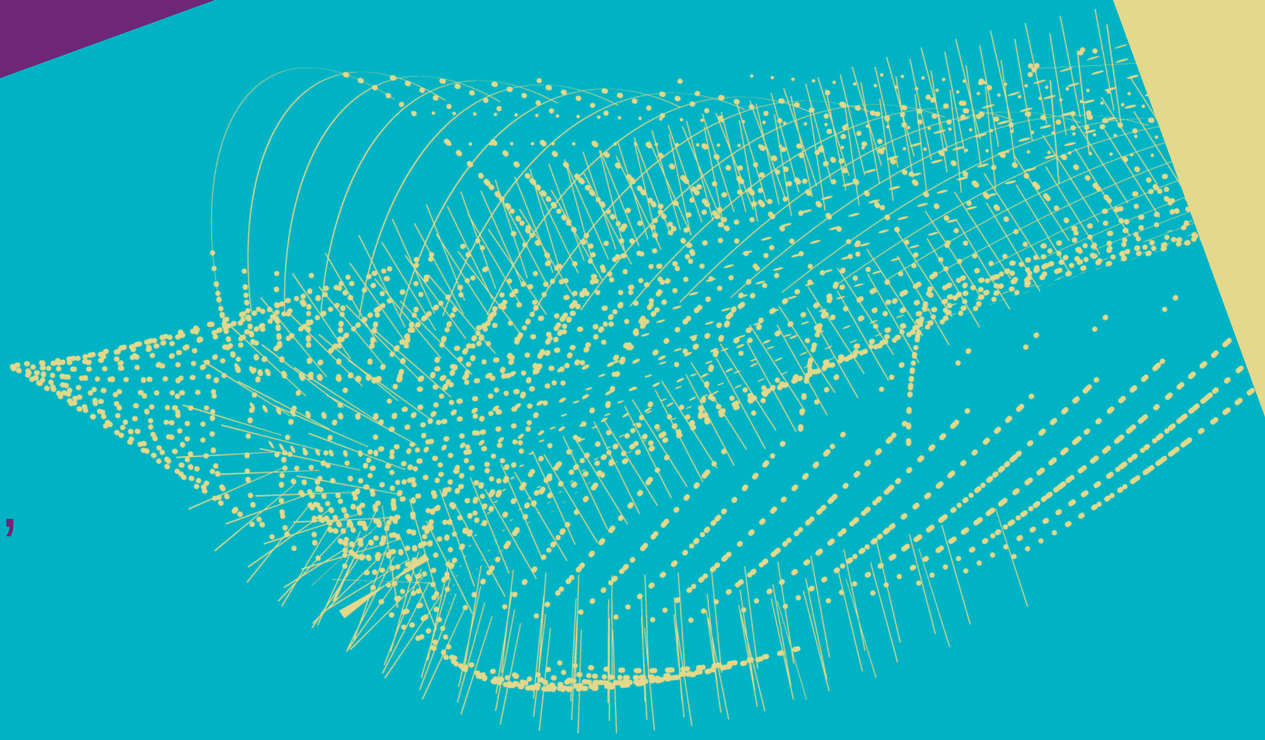
Nikhef



Michael Naafs, Guido Visser,
Pascal Bos

PROGRESS ON mmWAVE DOWNCONVERSION

Oct. 7th 2022

SCOPE OF RF DESIGN

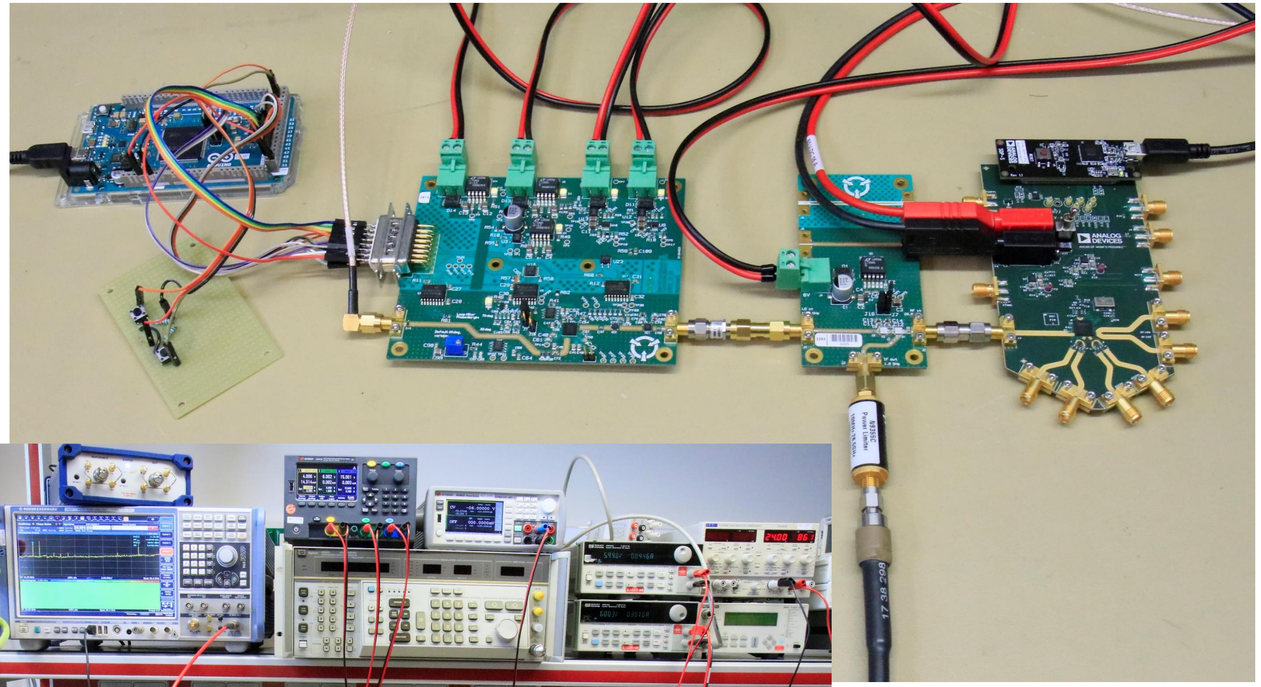
Normally:

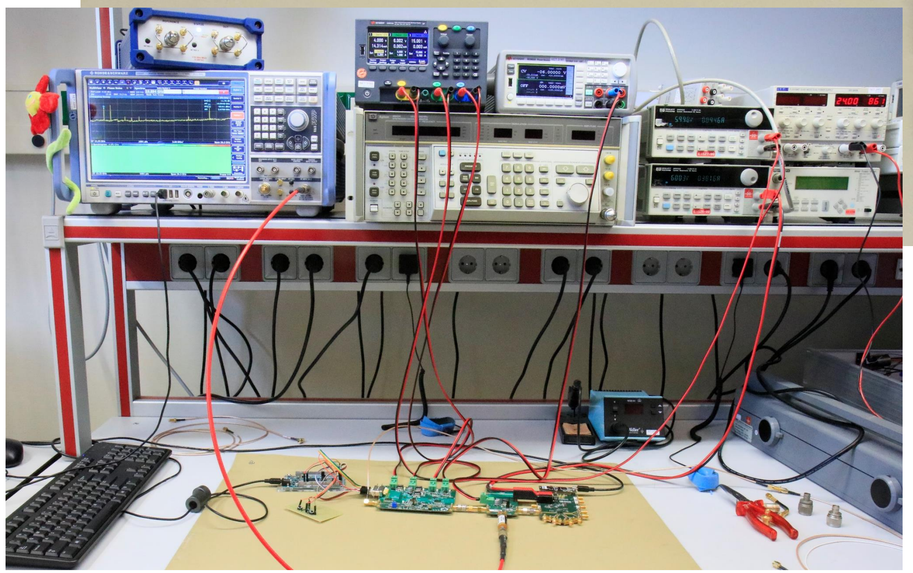
- Antenna
- Cryogenic amplifier(s)
- Down conversion

At Nikhef:

- Focus on down conversion and digitization

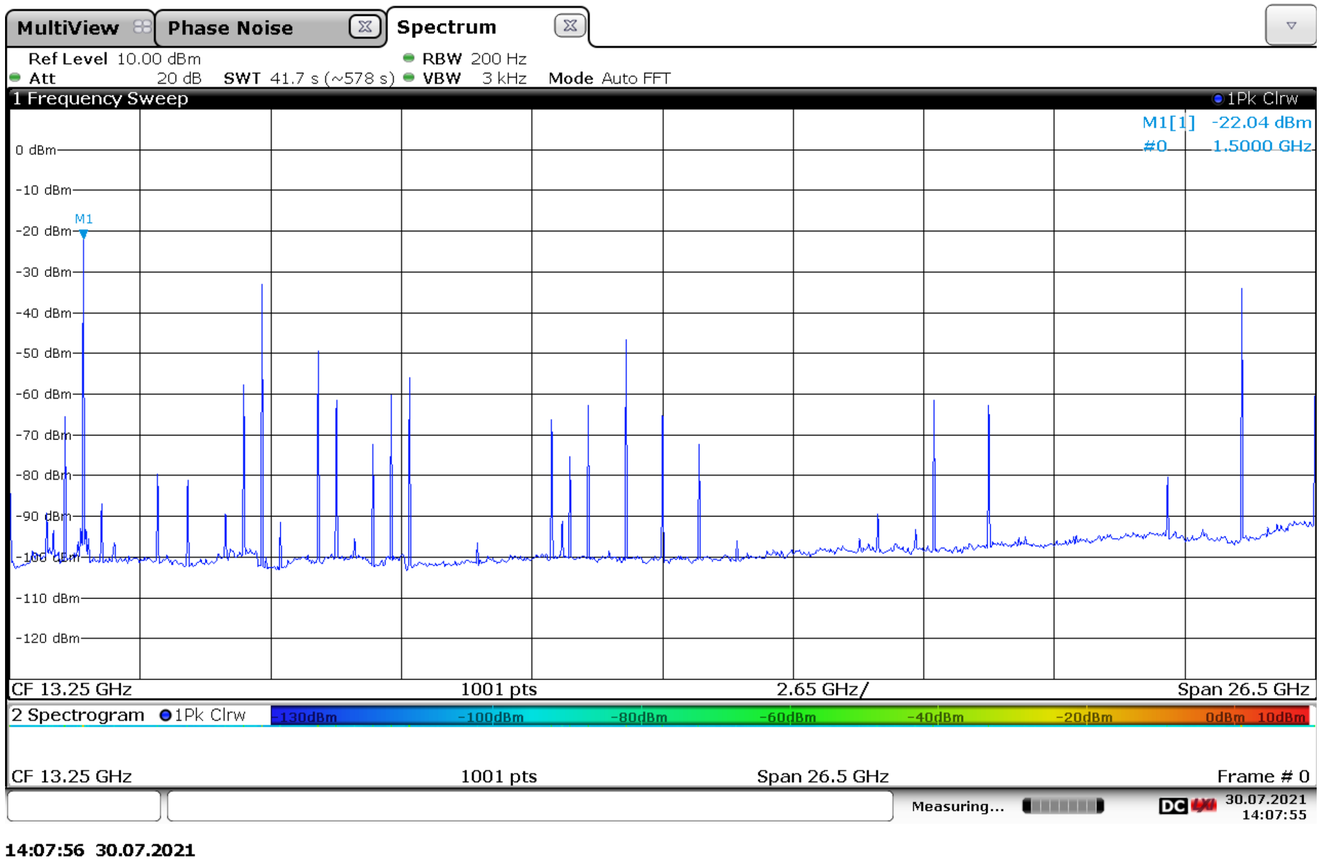
BABY STEPS (2021)





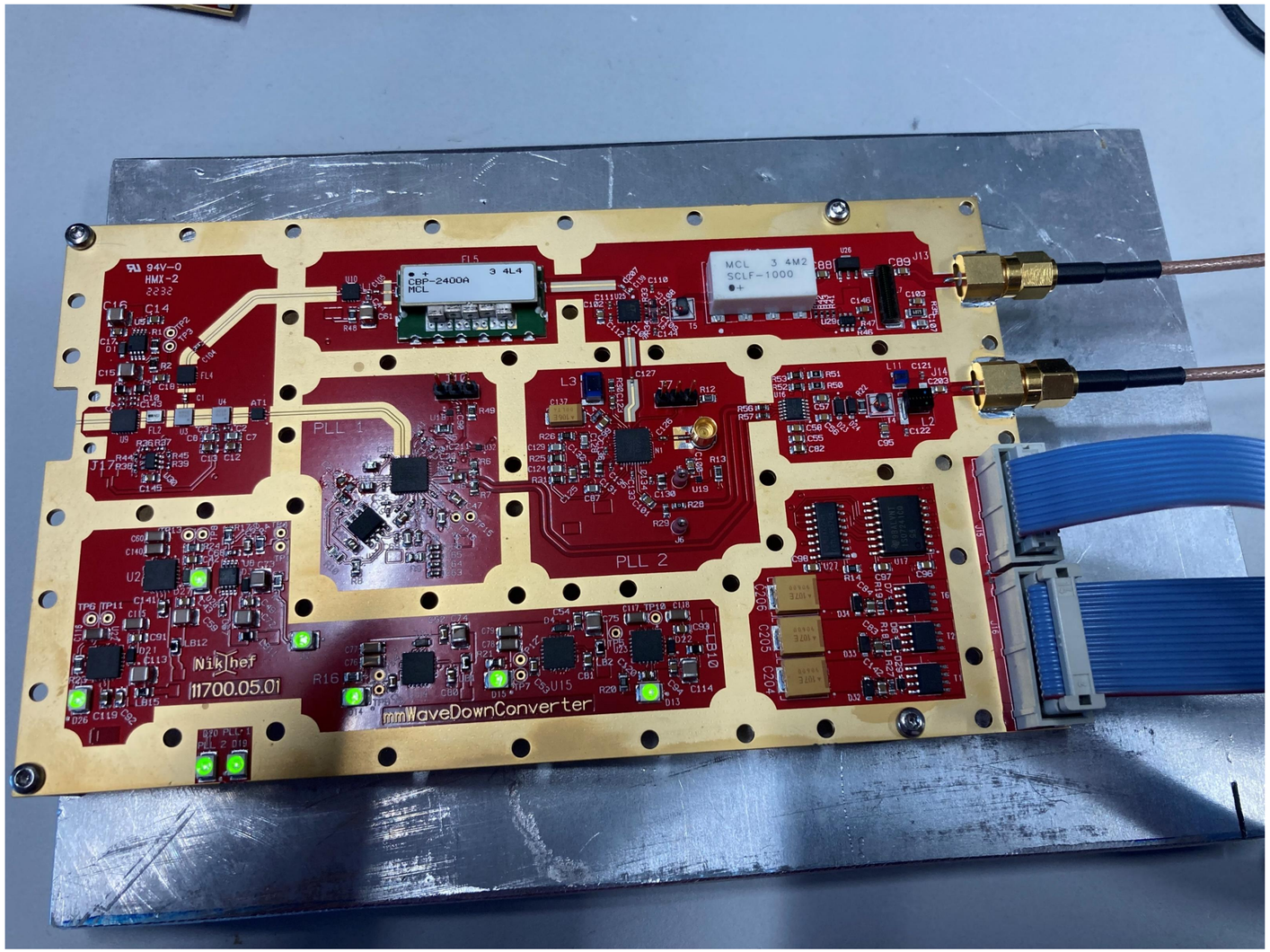
- Design of two PCBs
- Preliminary tests

BABY STEPS – LESSONS LEARNED



- Working proof of concept
- Valuable design experience @ Nikhef
- Foundation of work presented today

TODAY’S BOARD



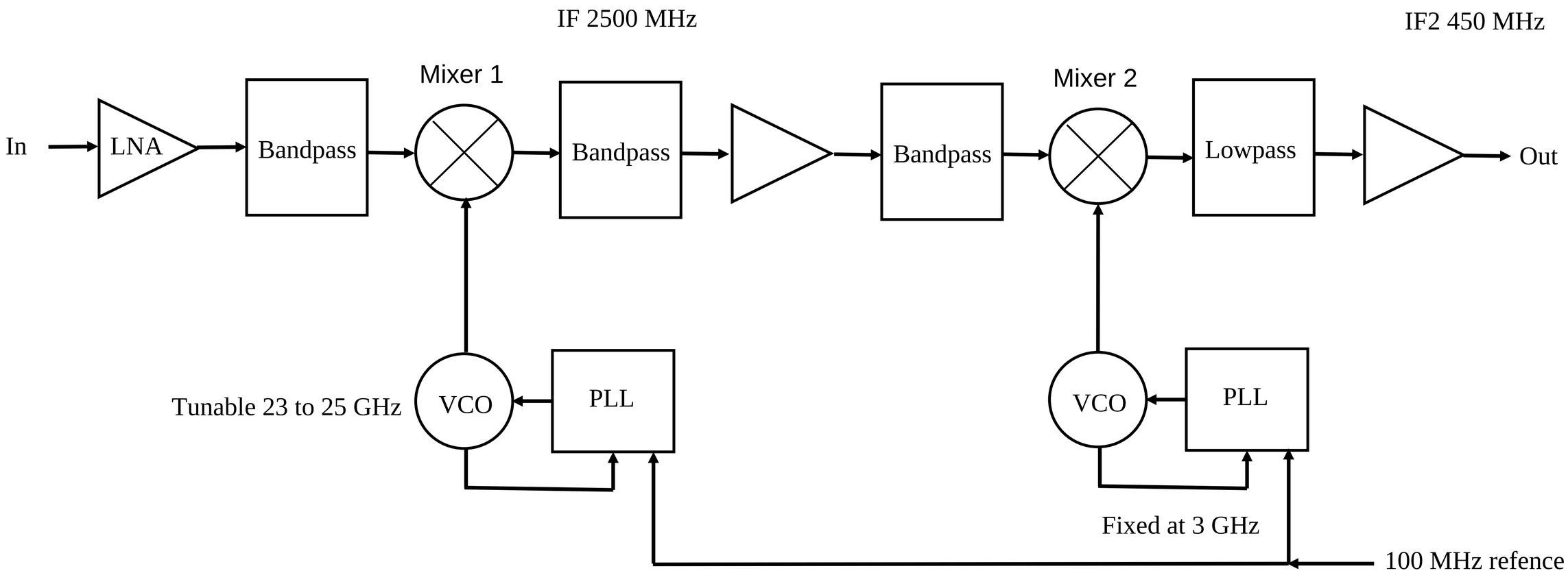
- Target Specs
- Block diagram
- Route to prototype
- The Prototype arrived
- Measurements
- Planned measurements
- Digitization
- What’s next?

TARGET SPECS

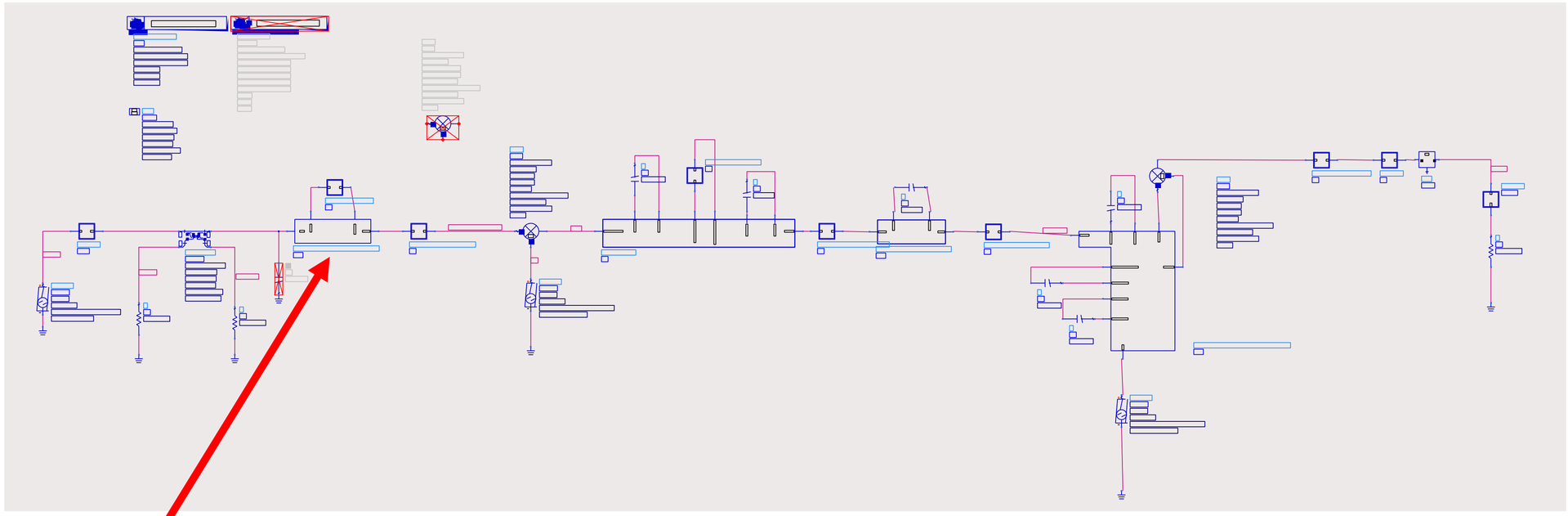
- Input range ~ 25.5 to 27.5 GHz
- Total conversion gain 60 to 65 dB
- Noise Figure 4.5 dB
- First IF 2500 MHz, Final IF 450 MHz

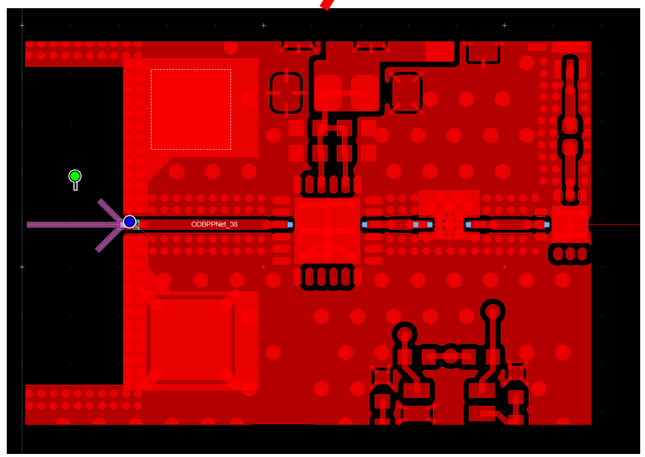
- Input return loss better than -10 dB (→S_{11} ≤ -10dB)
- Output return loss better than -15 dB (→S_{22} ≤ -15dB)
- External refence for the PLLs 100 MHz

BLOCK DIAGRAM



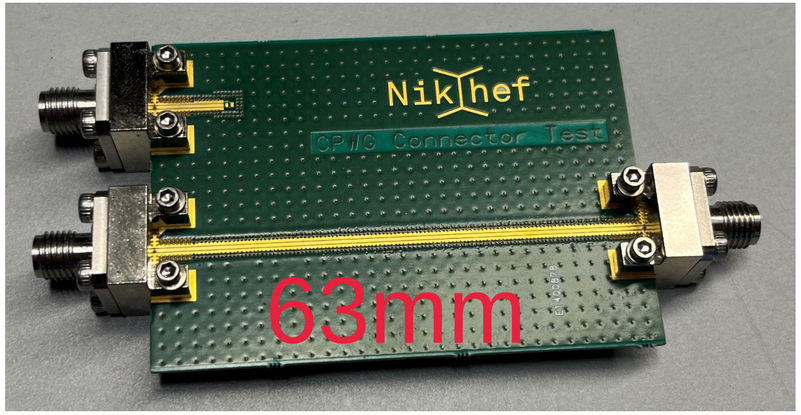
ROUTE TO PROTOTYPE: SIMULATION



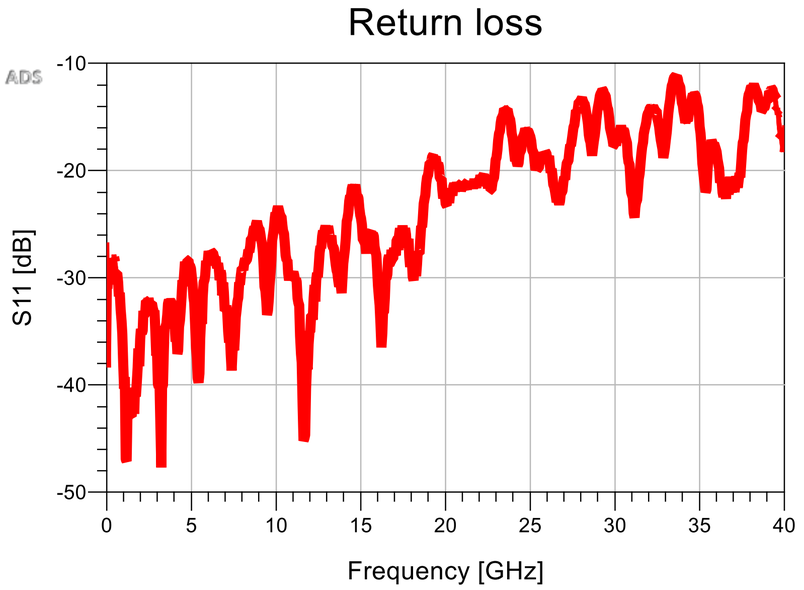


- LNA and Filters are “S-parameters blocks”
- Freq in 26.5 GHz
- Freq Out 450 MHz
- Simulated gain 58 dB (including layout effects)

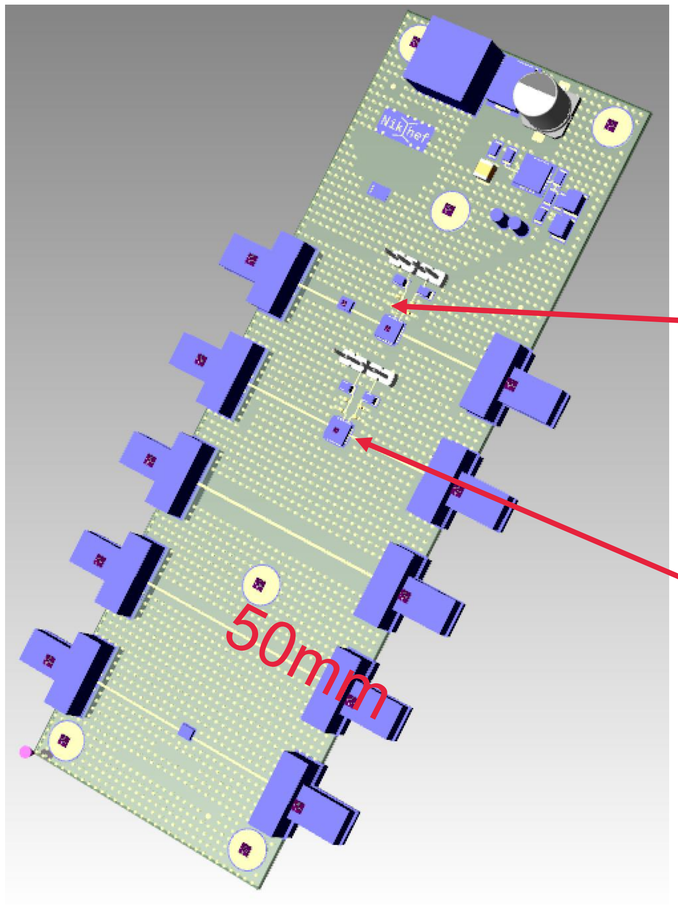
ROUTE TO PROTOTYPE: MEASUREMENTS

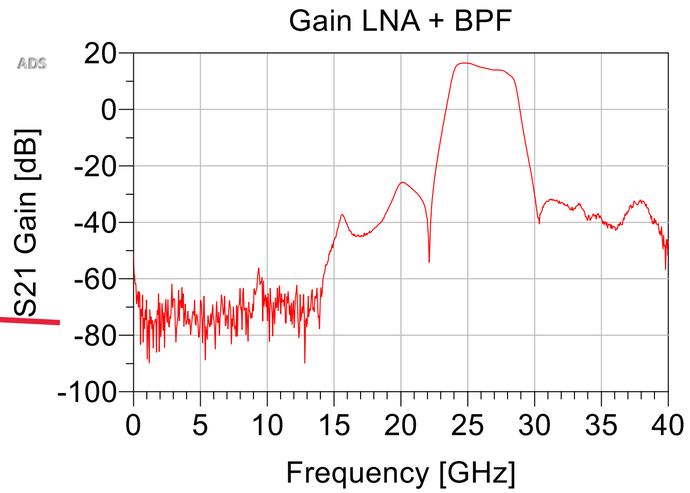


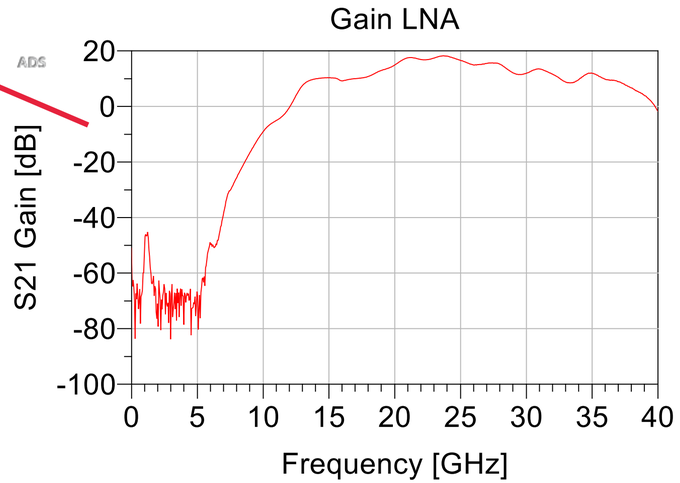
- Test PCB for connectors and transmission lines
- Nickel is unwanted
- Surface roughness
- Measured S-parameters



ROUTE TO PROTOTYPE: MEASUREMENTS (2)

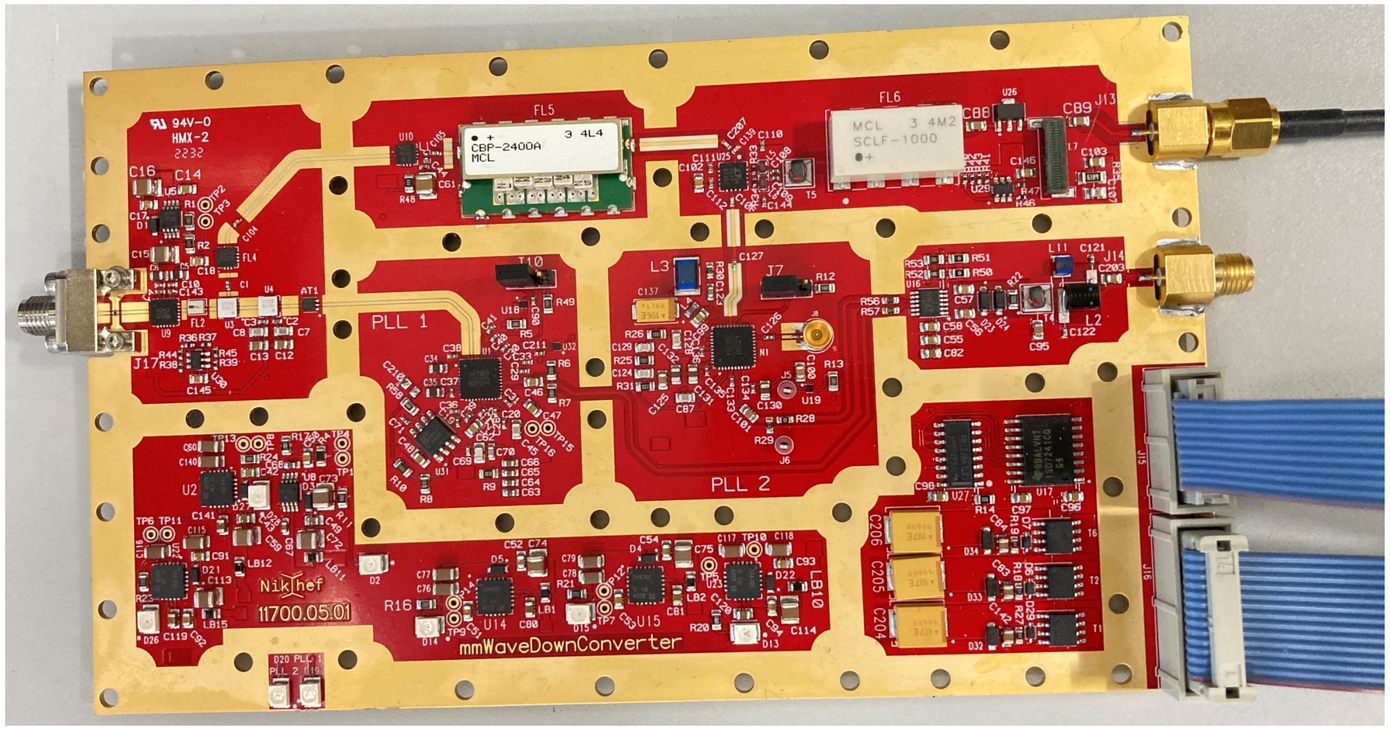






- Test PCB for
  1. transmission lines
  2. Connector to PCB transition
  3. BPF
  4. LNA + BPF
  5. LNA

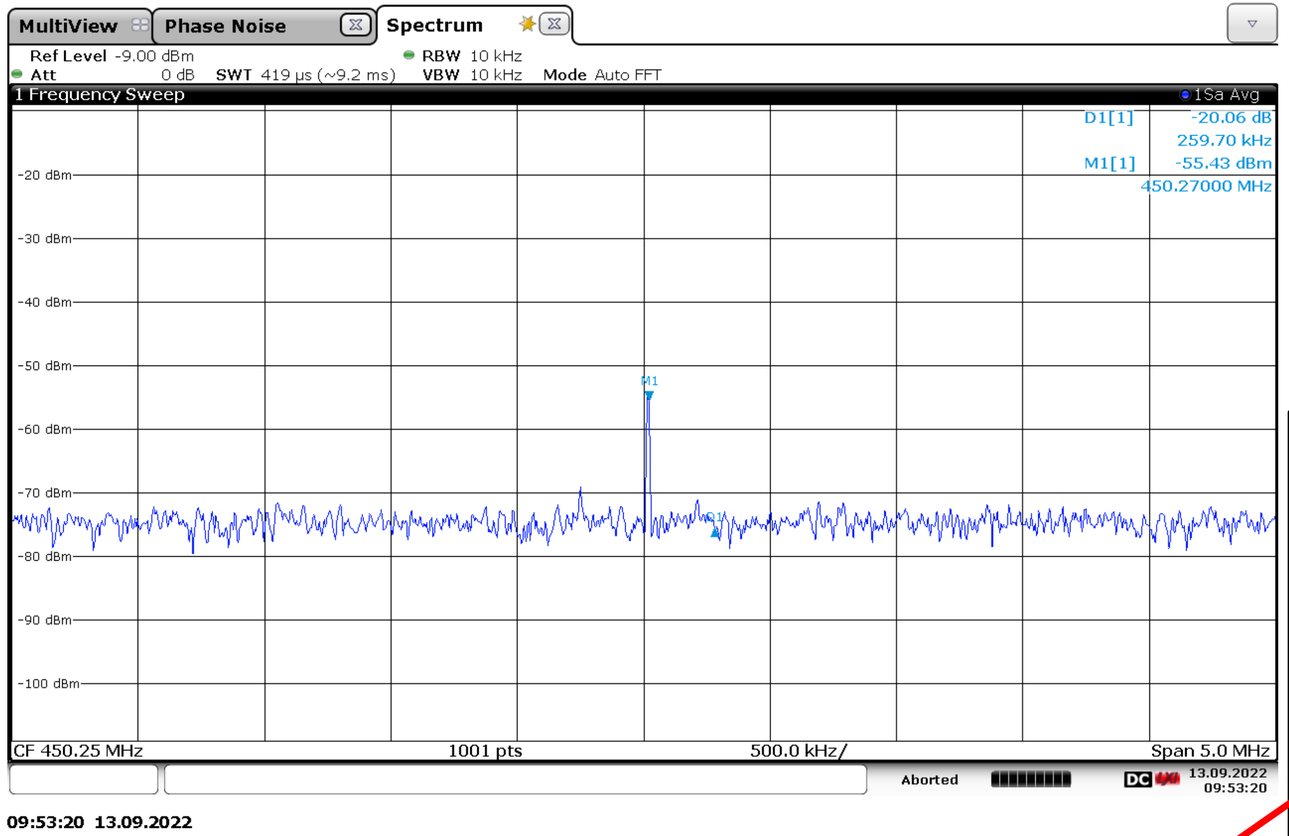
THE PROTOTYPE ARRIVED



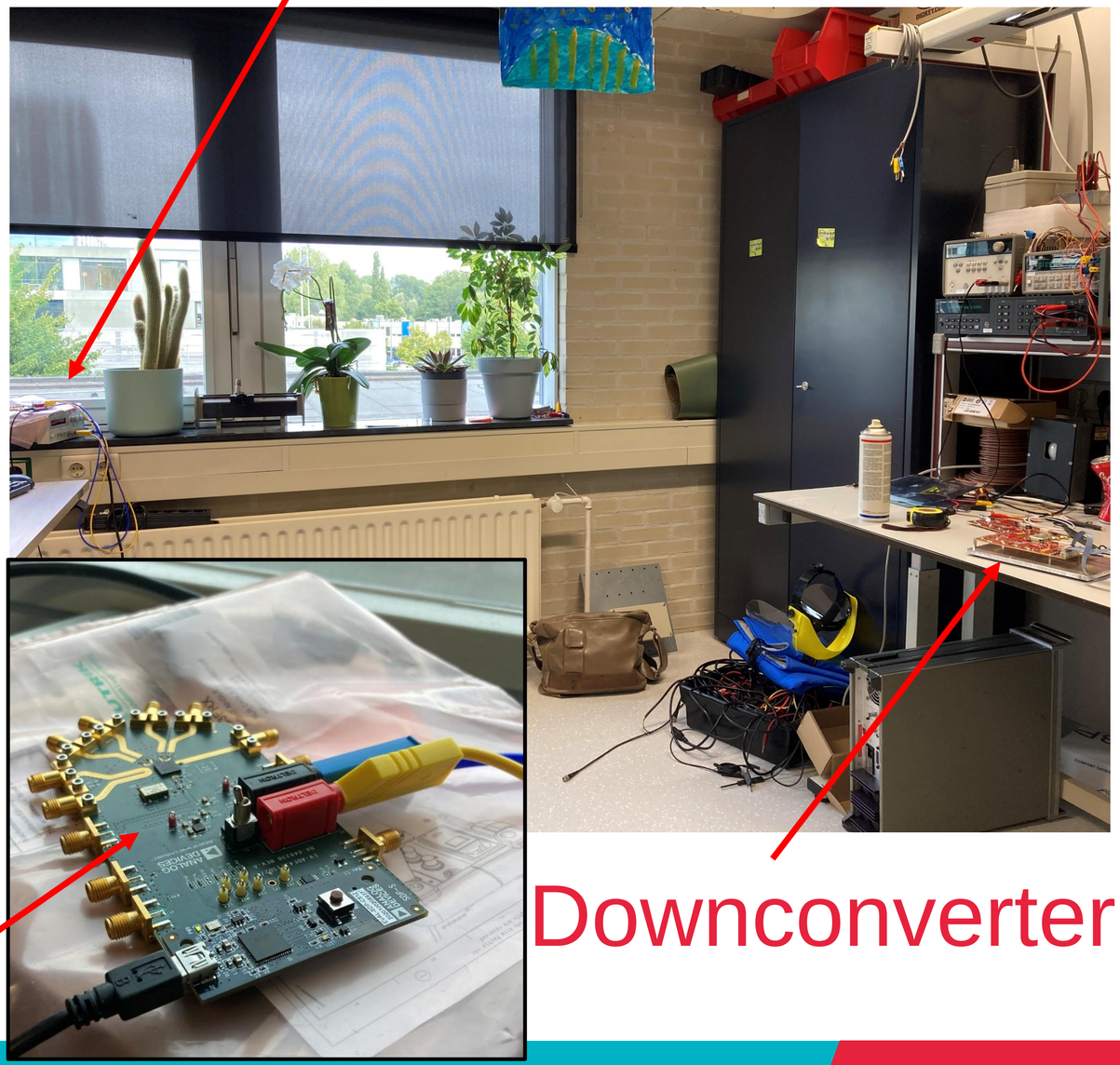
- Left: RF input connector
- Right (top to bottom): Output, Ref in, control, power

“FIRST LIGHT”

- Downconversion works



Source (26.5GHz)

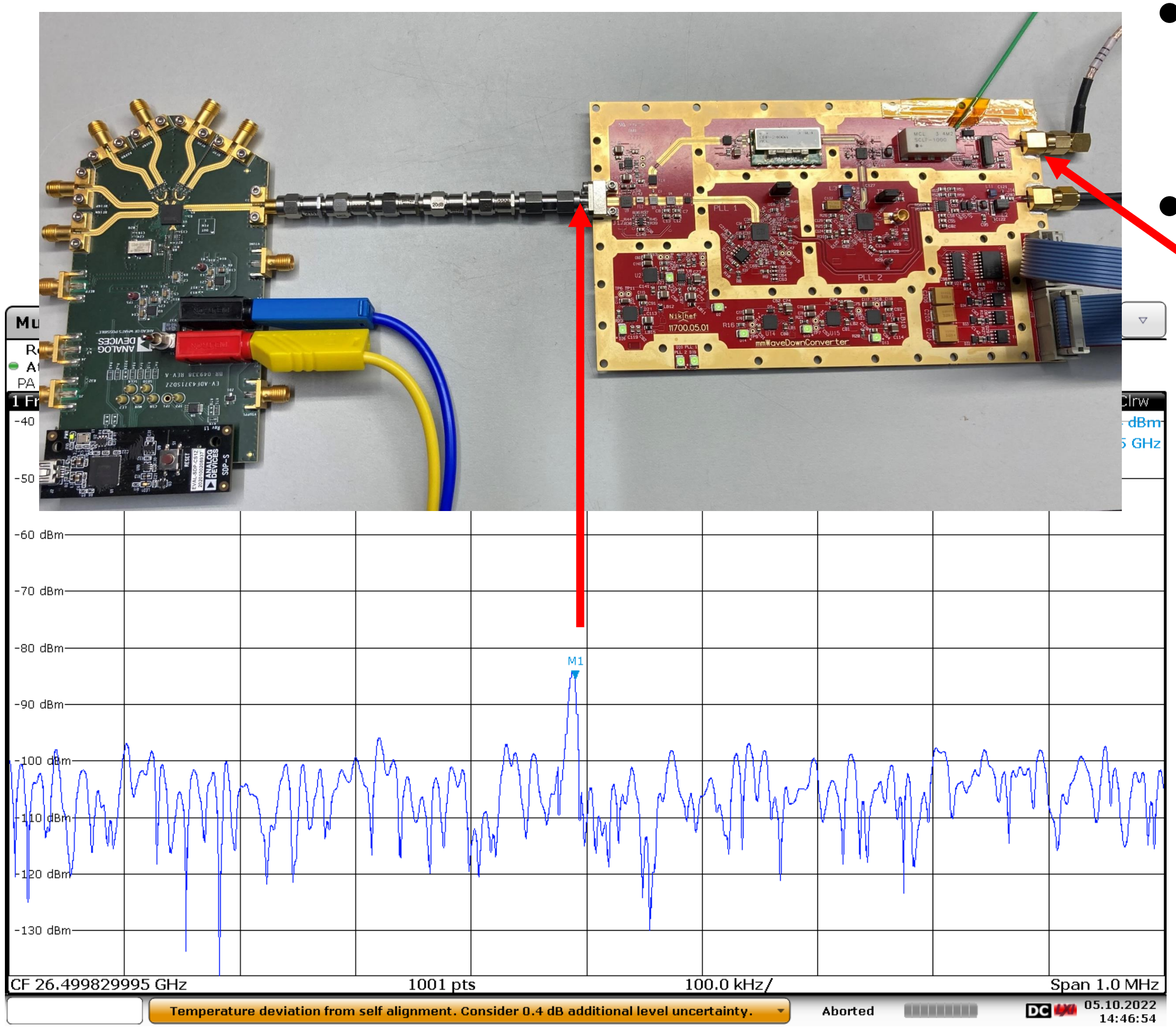


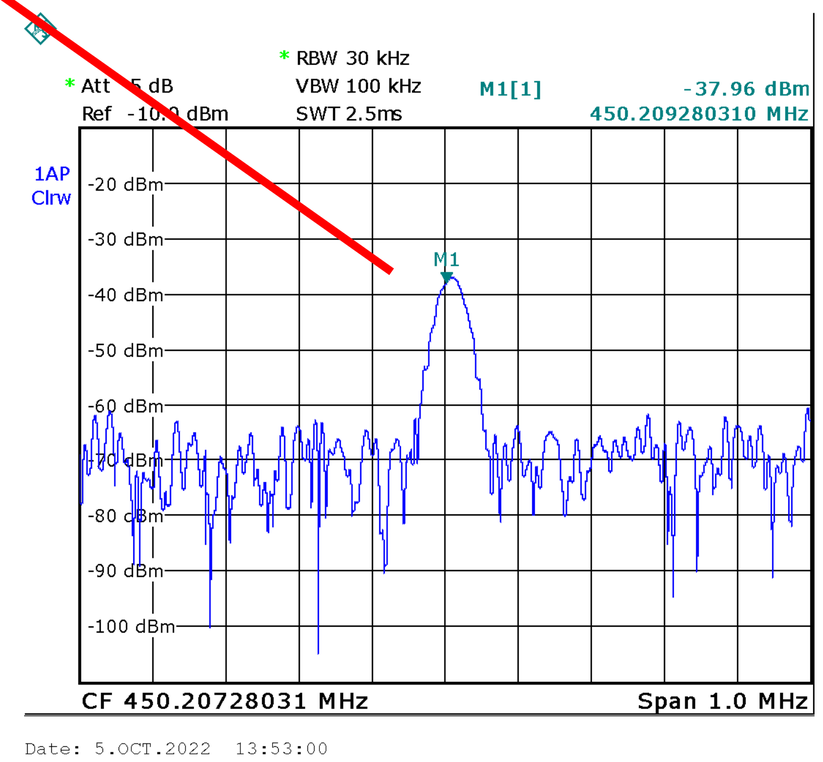
Source (26.5GHz)

Downconverter

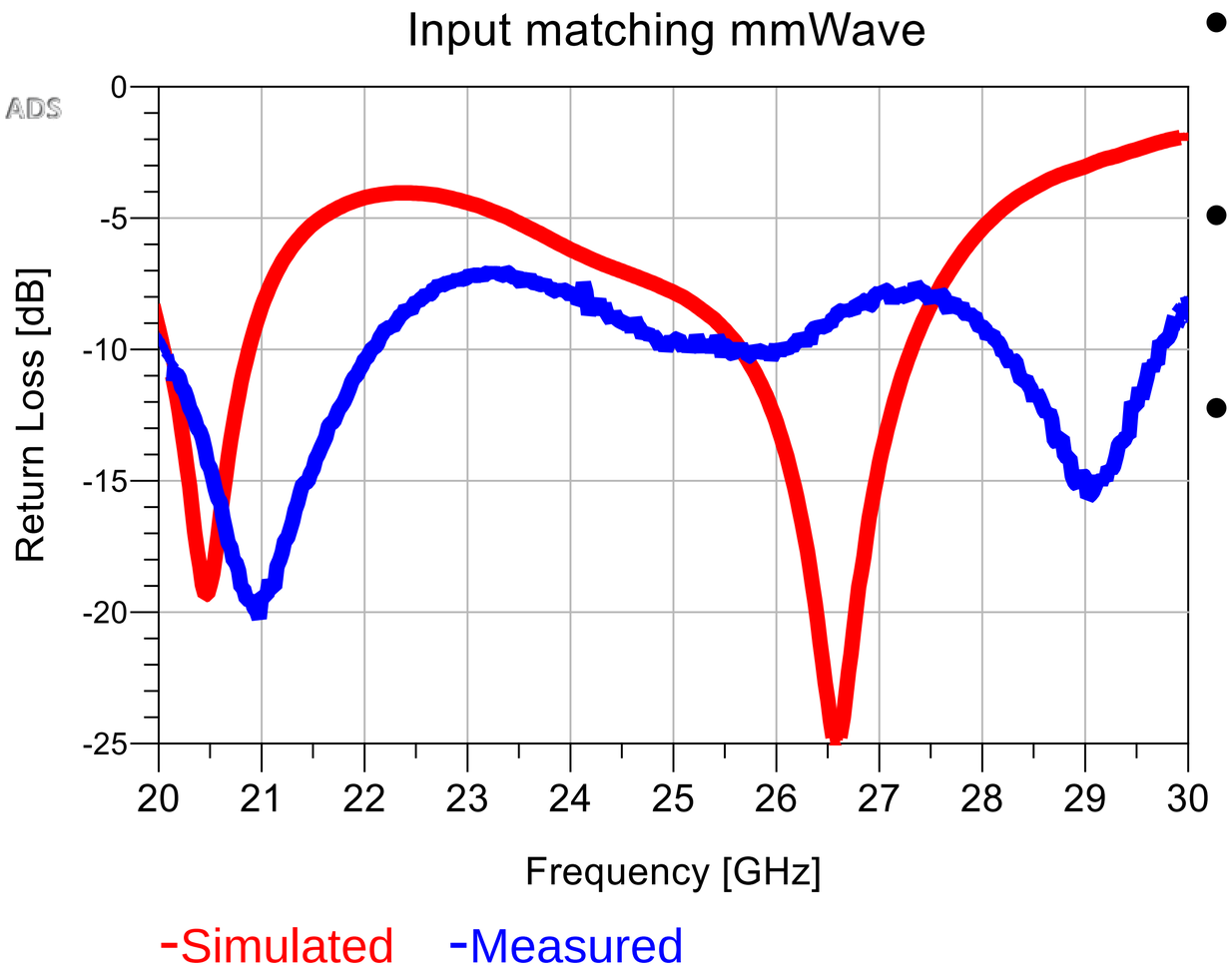
MEASUREMENTS - CONVERSION GAIN

- Gain < expected (~45dB instead of 60dB)
- High measurement uncertainty

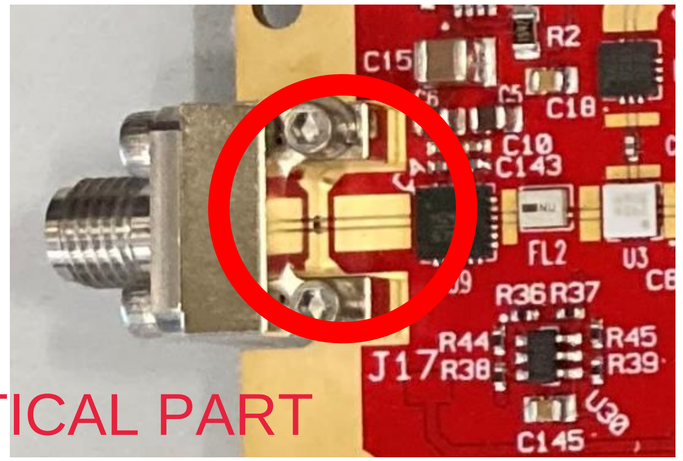




MEASUREMENTS – INPUT MATCHING

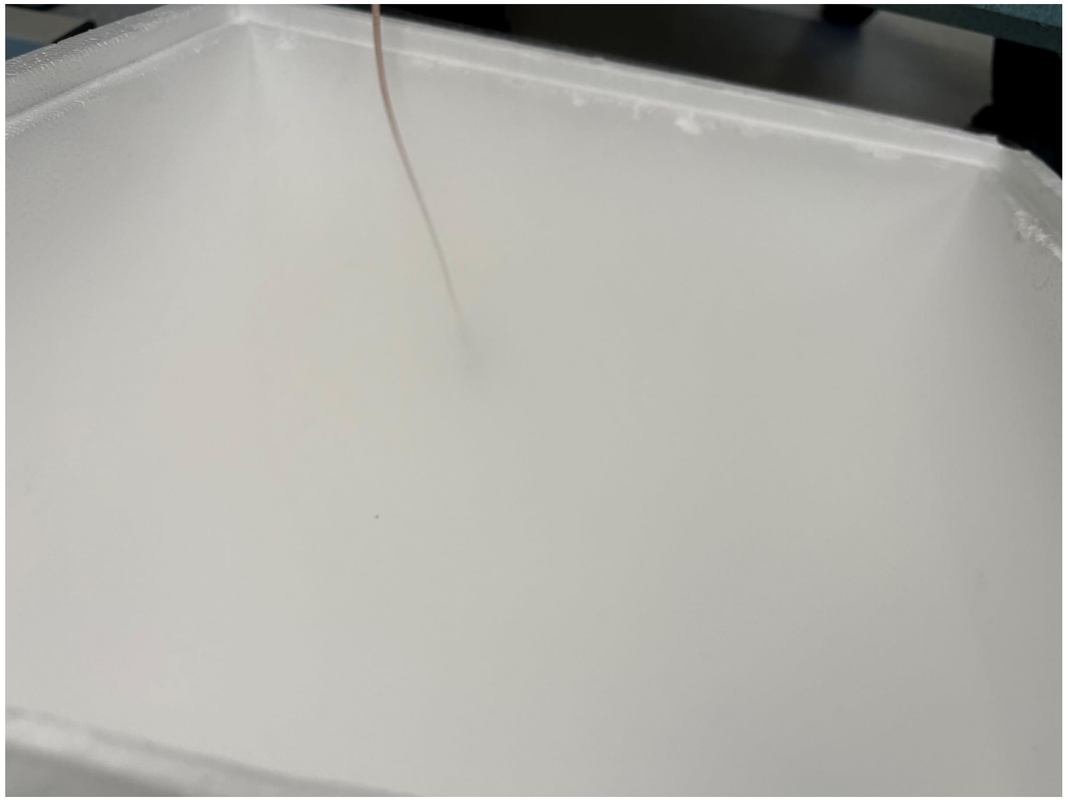


- LNA (mis)match shape recognisable
- Mismatch should be dominated by LNA
- Connector – PCB transition should be better



CRITICAL PART

PLANNED MEASUREMENTS

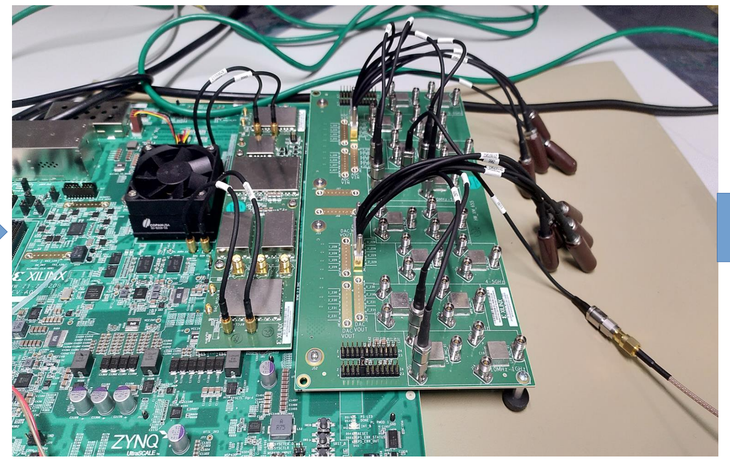


- Measure the frequency response and gain properly
- Maybe: measure individual components (de-embedded)
- Measure the noise figure

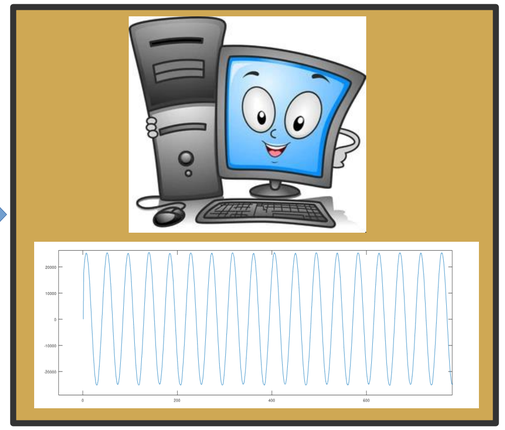
DIGITIZATION – WHAT WE CAN DO

- Set sample clock to 5GHz
- Configure / setup the ADC and DAC
- Readout via FPGA's internal analyser (JTAG)
- Setup a Linux environment for future house keeping

Sine wave



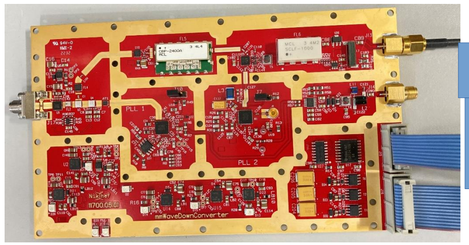
JTAG



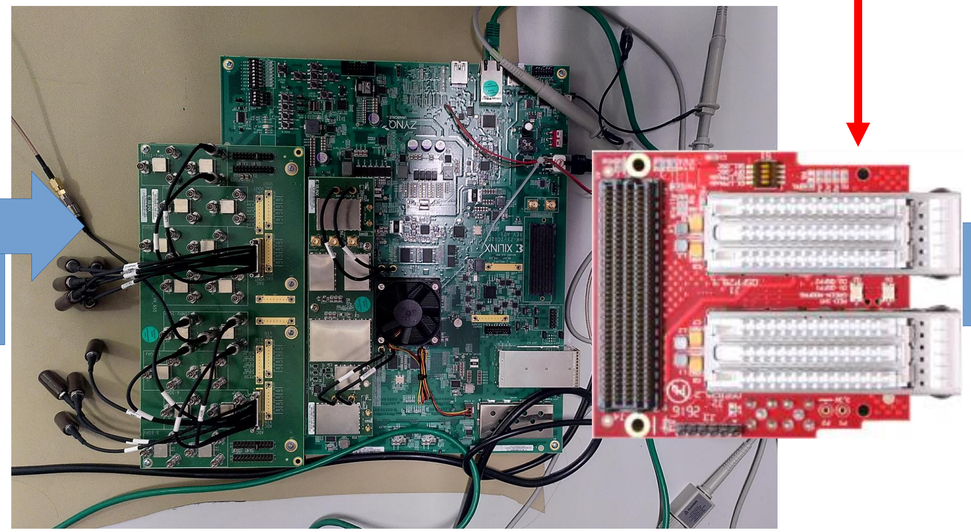
FPGA: ZYNQ ULTRASCALE+
RF SOC ZCU208

DIGITIZATION – WHAT WE WANT TO DO

- Readout at 5Gsps via 100GbE with RDMA
- Read raw ADC data on PC-side for algorithm development
- Buy some new HW to make this possible
- Run Doom on it :)

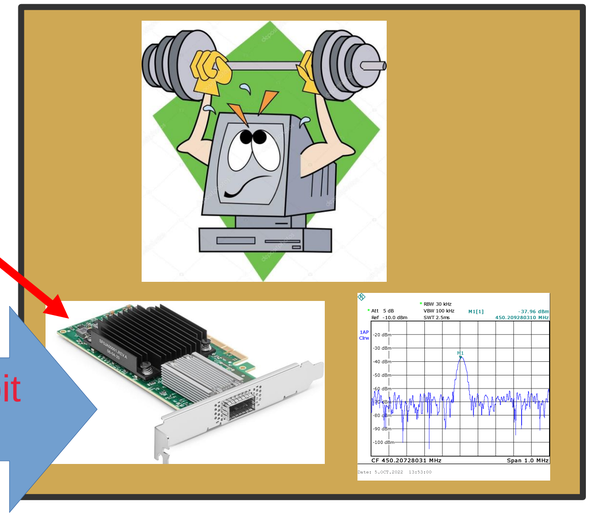


IF-signal

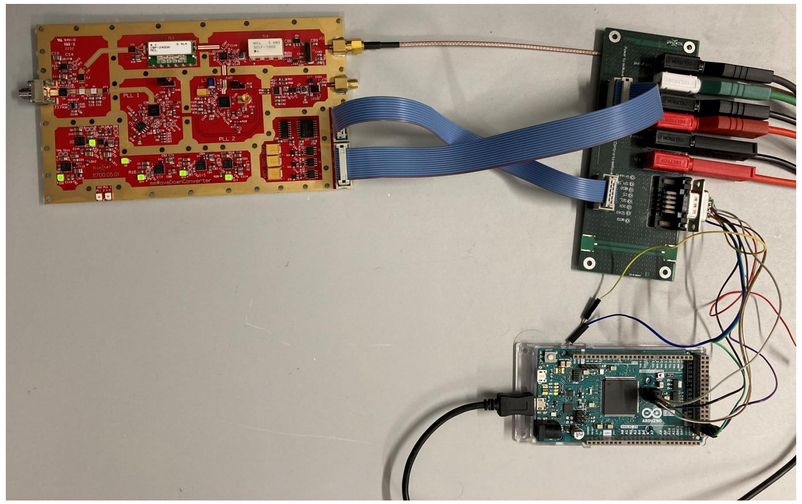


FPGA: ZYNQ ULTRASCALE+
RFSoC ZCU208

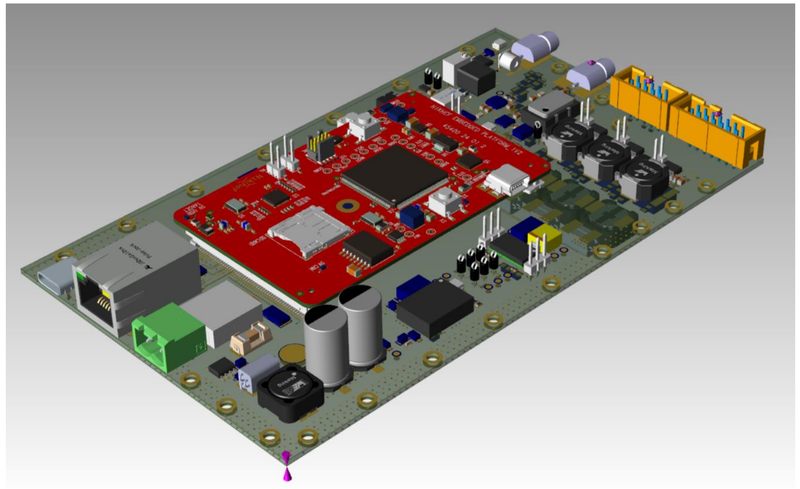
2x 100 Gigabit Ethernet

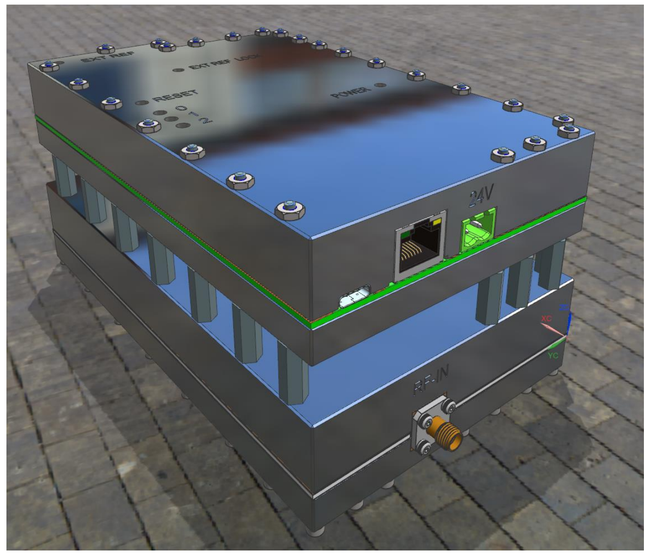


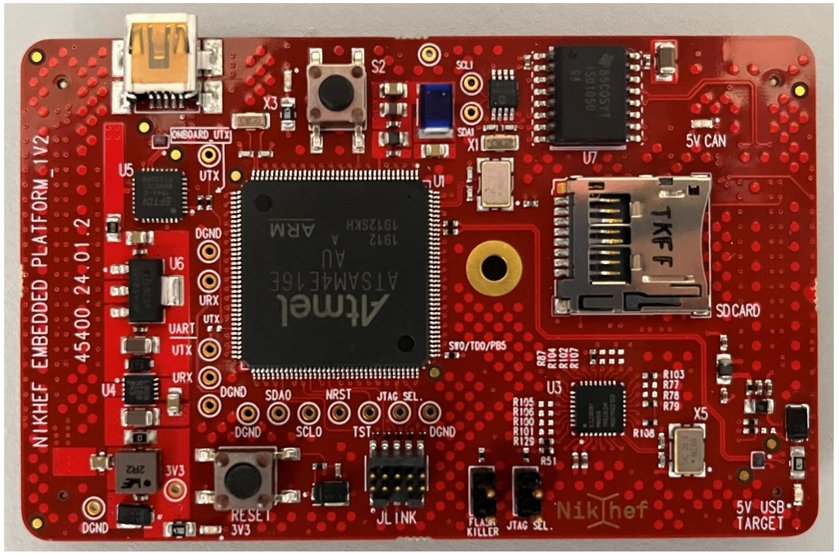
WHAT'S NEXT?



- Setup / control is clumsy and fragile
  → Controller PCB
- Metal case
- Controller software development (NEP)
- FPGA firmware development
- Closing the signal chain







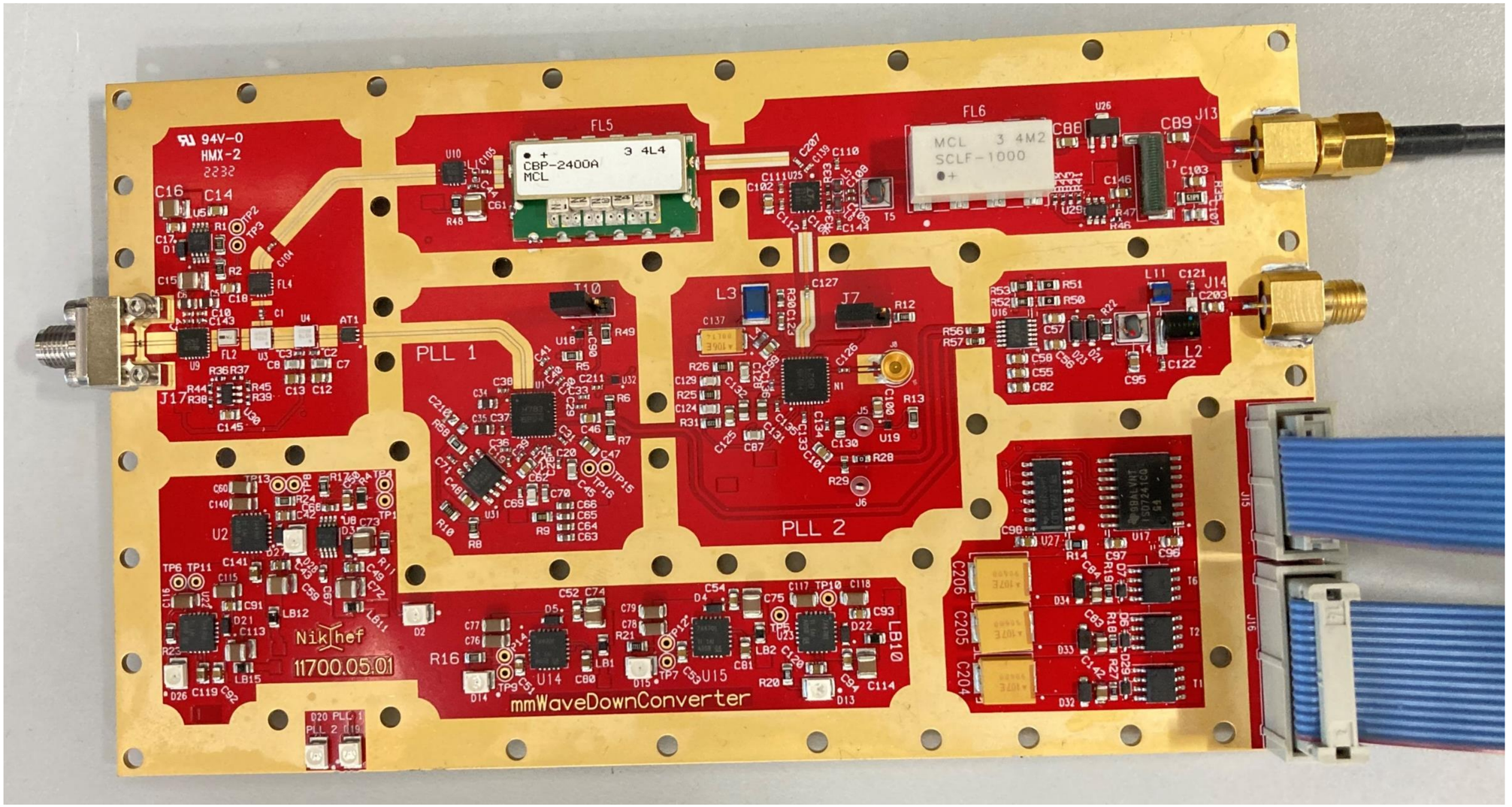
WHAT'S NEXT? (2)

VNA

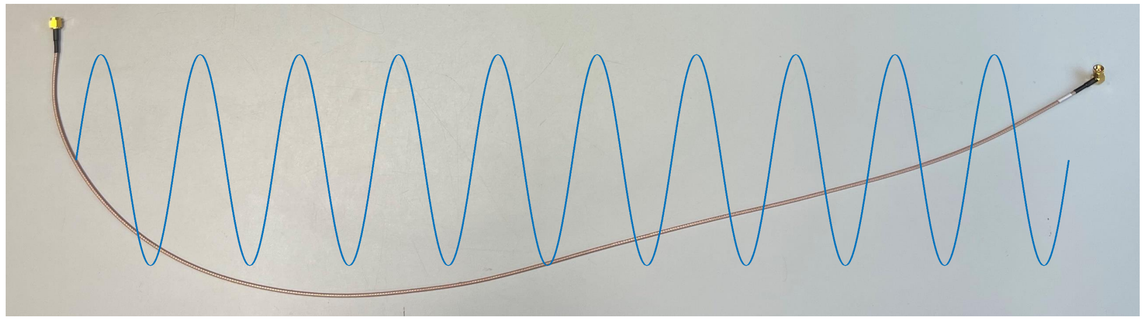
- Obsolete components → redesign
- Different requirements (e.g. BW, IF, etc.)
- Lessons learned from this prototype
- Now practically blind & mute above 20GHz
  → Setup proper measurement system
- Very expensive

Low level signal generator

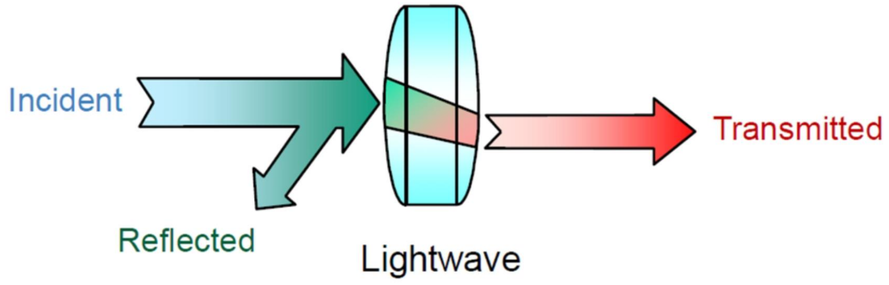
QUESTIONS / SUGGESTIONS?

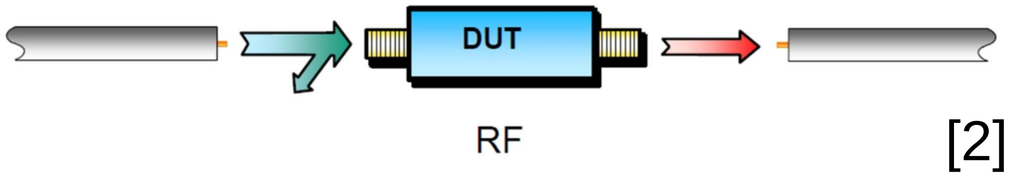


RF DESIGN 101



- What is RF design
- Component size large compared to wavelength
- ~~Voltage~~ / ~~current~~
- Power and S-parameters





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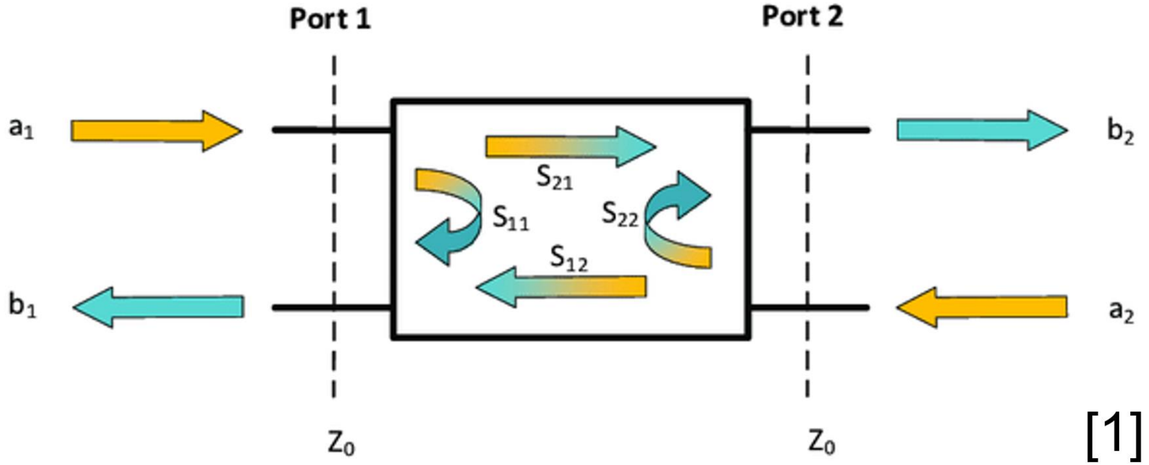

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