ATLAS HGTD Demonstrators

NNV Annual meeting - Lunteren
Parallel session Ic

Marion Missio for the HGTD collaboration

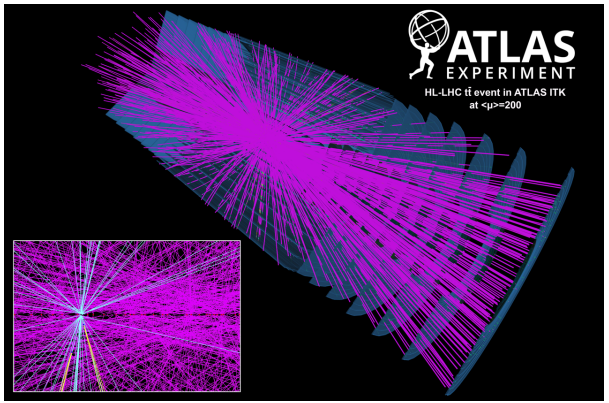
04 November 2022

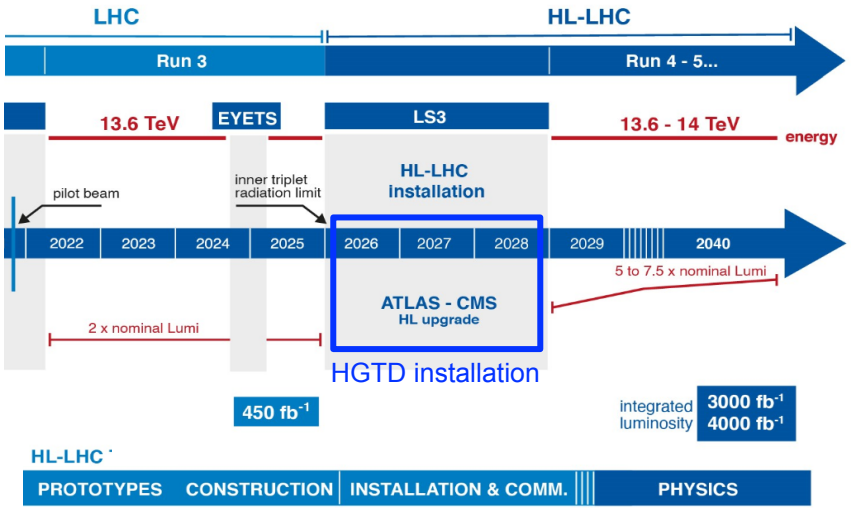
The high-luminosity LHC (HL-LHC)

HL-LHC :

- start in 2029
- significant increase in number of interactions = increase the LHC potential

- give access to rare events (dark matter, physics beyond the SM)
- allow measurements with better precision and sensitivity

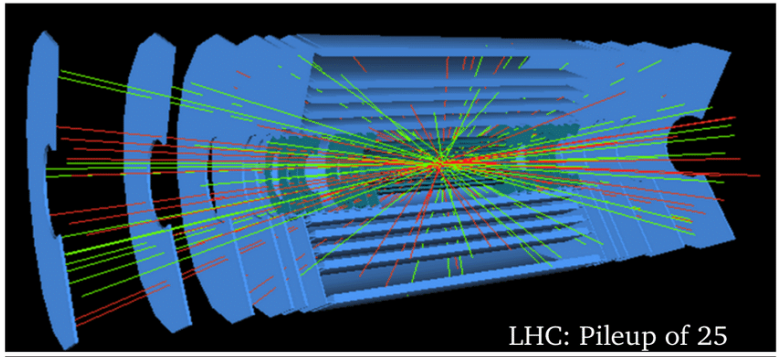


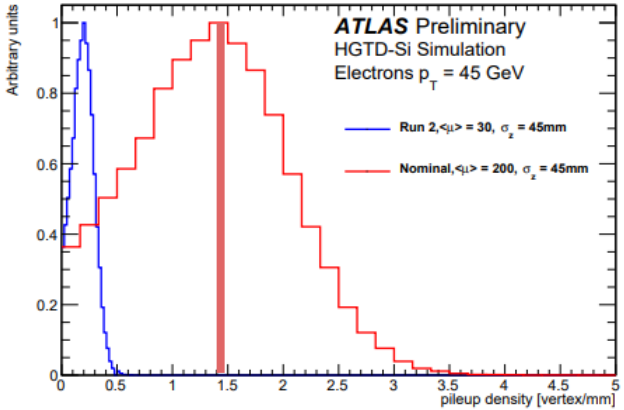


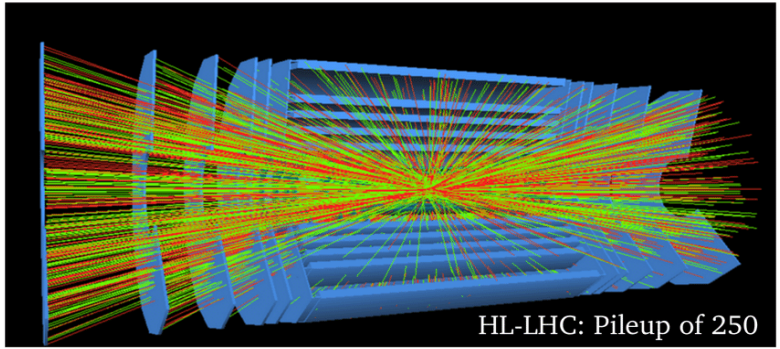
HL-LHC : dealing with high event rate

Will be challenging :

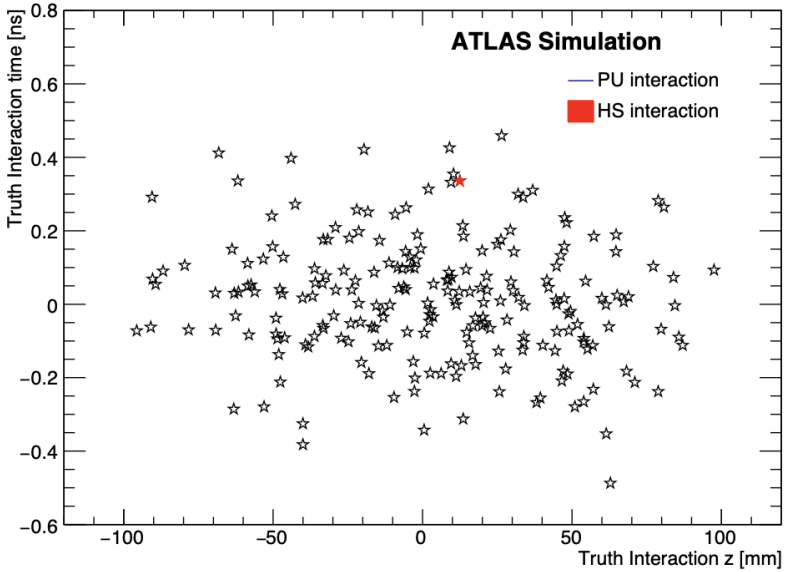
- significant increase in the statistics available ➡ high particle densities
- Pileup = 200 (~35 for Run2) proton-proton collisions per bunch crossing ➡ ~1.5 vertices/ mm
- high radiation environment



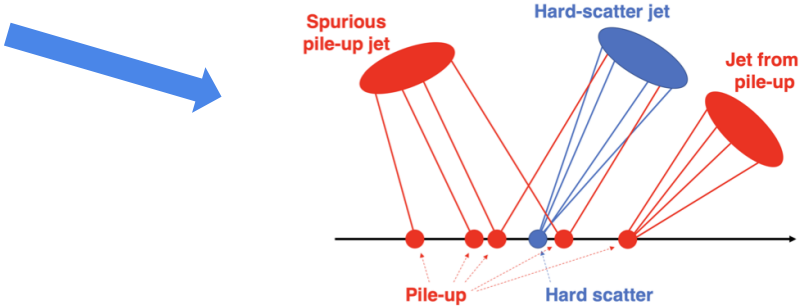




HL-LHC : dealing with high event rate



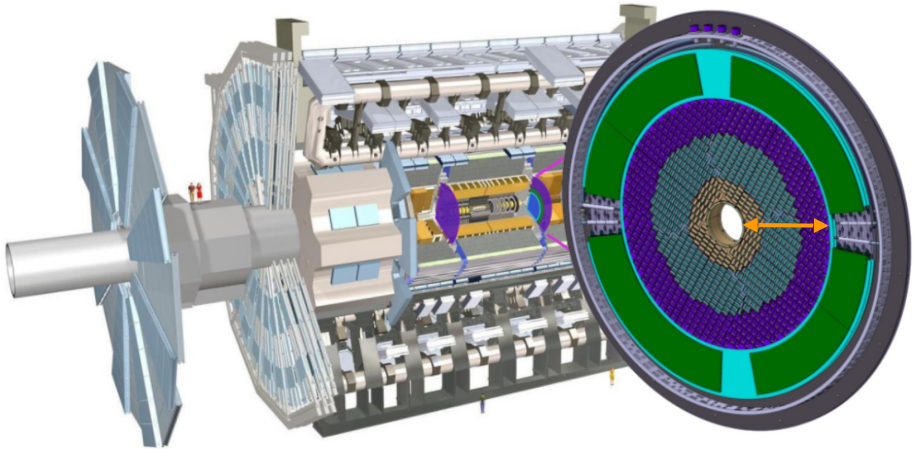
- Pileup interaction ☆ can add jets or alter the properties of hard-scatter jet = degrade the physics performance
- One of the biggest challenges is to separate collisions very close in space
- The ATLAS detector requires a major update

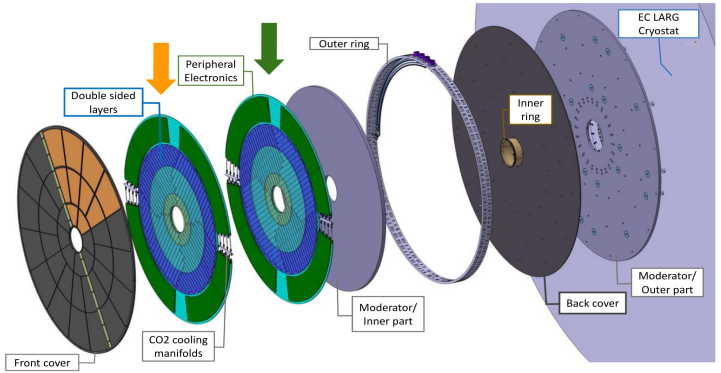


The High Granularity Timing Detector (HGTD)

The HGTD will reduce pileup and provide time measurement in the forward region

- Two disks located between the barrel and the end-cap calorimeter (at z ± 3.5m)
- Target time resolution : 30-50ps per track
- Active area : 2.4 < |η| < 4.0, **12 < R < 64 cm**





Two double-sided layers per disk :

- Sensors : **silicon LGADs** (Low Gain Avalanche Detector)
- Readout : **custom ASICs**

One layer for data transfer :

- **Peripheral electronic boards** mounted on the outer ring

HGTD : Hybrid modules

Hybrid modules :

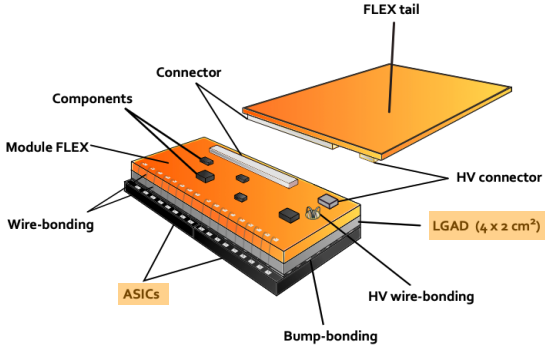
- Bare module : two LGAD sensors and two ASICs
- flexible printed circuit board (flex tail)

LGAD (Low Gain Avalanche Detector) :

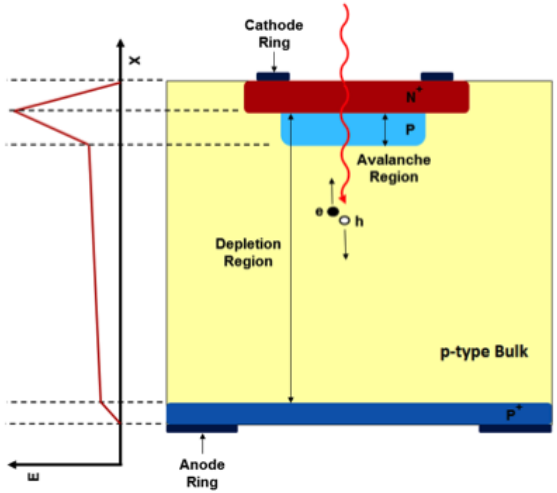
- standard **n-p** Si detector with **additional p-type doped layer** producing additional charge multiplication
- 15 x 15 pads (pad size : 1.3 x 1.3 mm²)

Custom ASIC :

- bump-bonded to the LGADs
- 15 x 15 readout channels
- Provides time of arrival (TOA) measurement



*not to scale

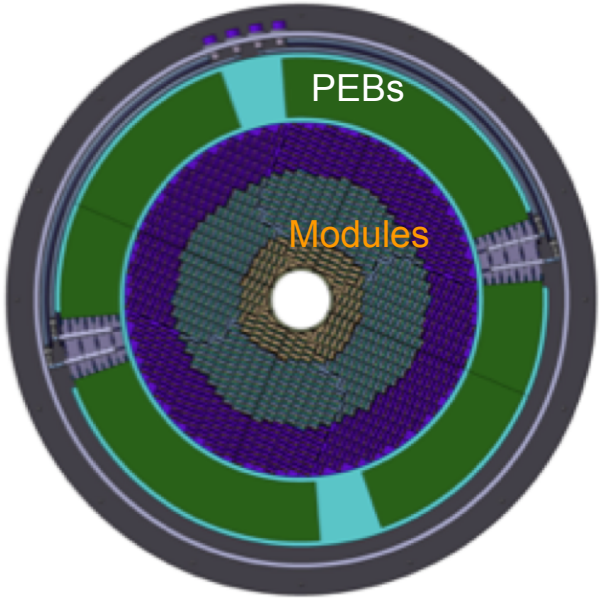


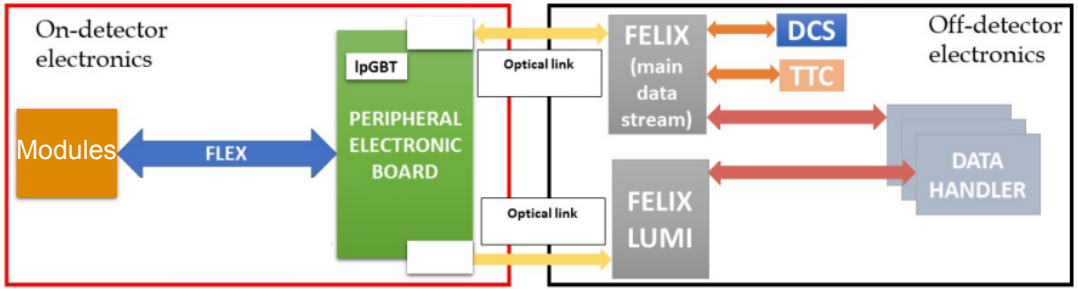
HGTD : Peripheral Electronics Boards

Data transfer :

- between hybrid modules and DAQ/Luminosity and Detector Control (DCS) systems
- via lpGBTs : CERN-developed radiation-tolerant data transmission ASICs
- and via FELIX (Front-End LInk eXchange) : main interface between the off-detector back-end and the on-detector electronics

Also control, monitor and distribute power supply





HGTD : Demonstrators

Goal : to validate aspects of the final design and integration

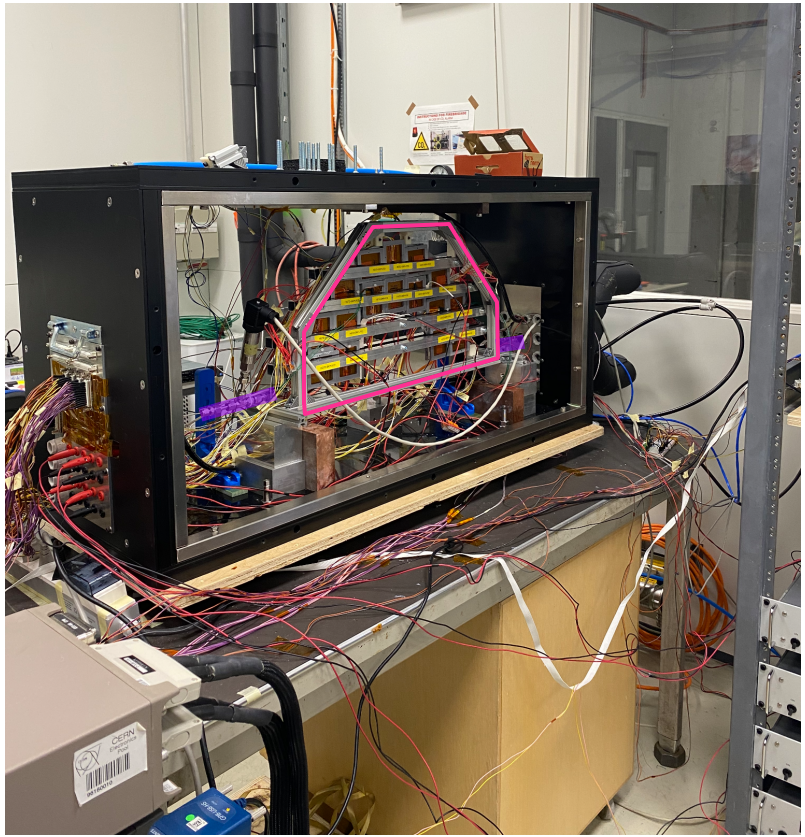
Two prototypes are being developed at CERN :

- **Heater demonstrator :** for mechanics and cooling aspects
- **DAQ demonstrator :** for electronics and readout aspects

HGTD : Heater demonstrator

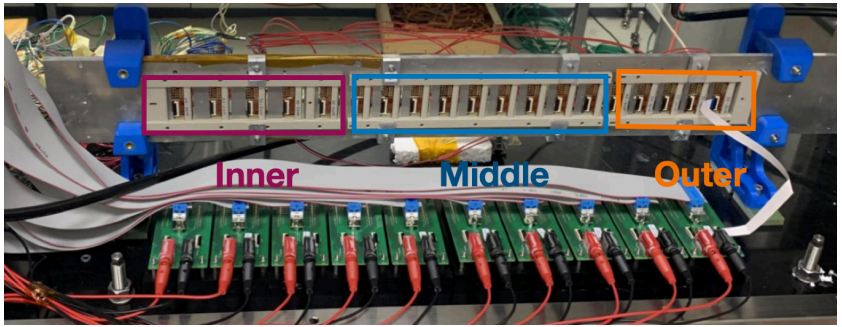
Goal : to develop the cooling of the detector and validate the module loading procedure

- Study the thermal stability
- Test different thermal materials to ensure a good thermal contact between the module and the support unit
- Validate the assembly procedures

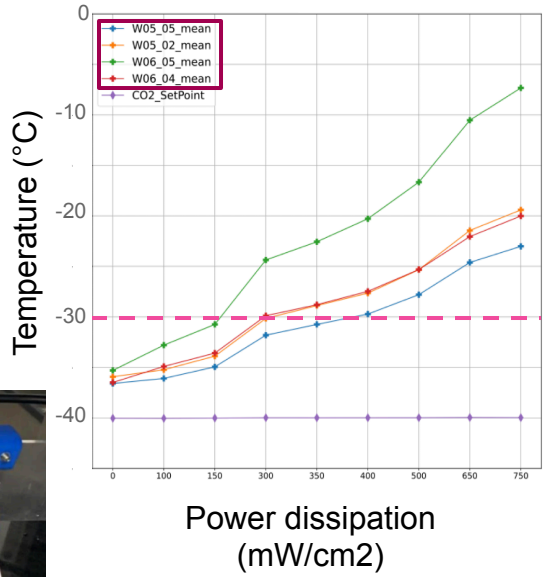


Heater demonstrator : Thermal stability

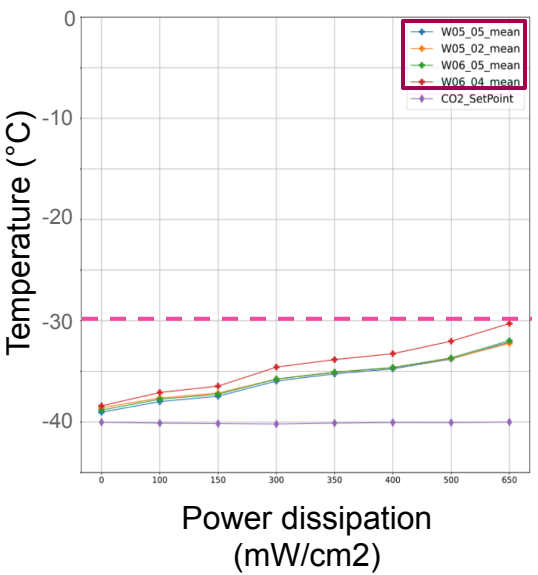
- Modules can have thermal runaway
- Silicon heater are used to simulate that
- Goal : find the setup to guarantee the most uniform cooling performance (sensors operate at **-30°C**)
    - can test different thermal materials, material for cooling plate



No thermal material



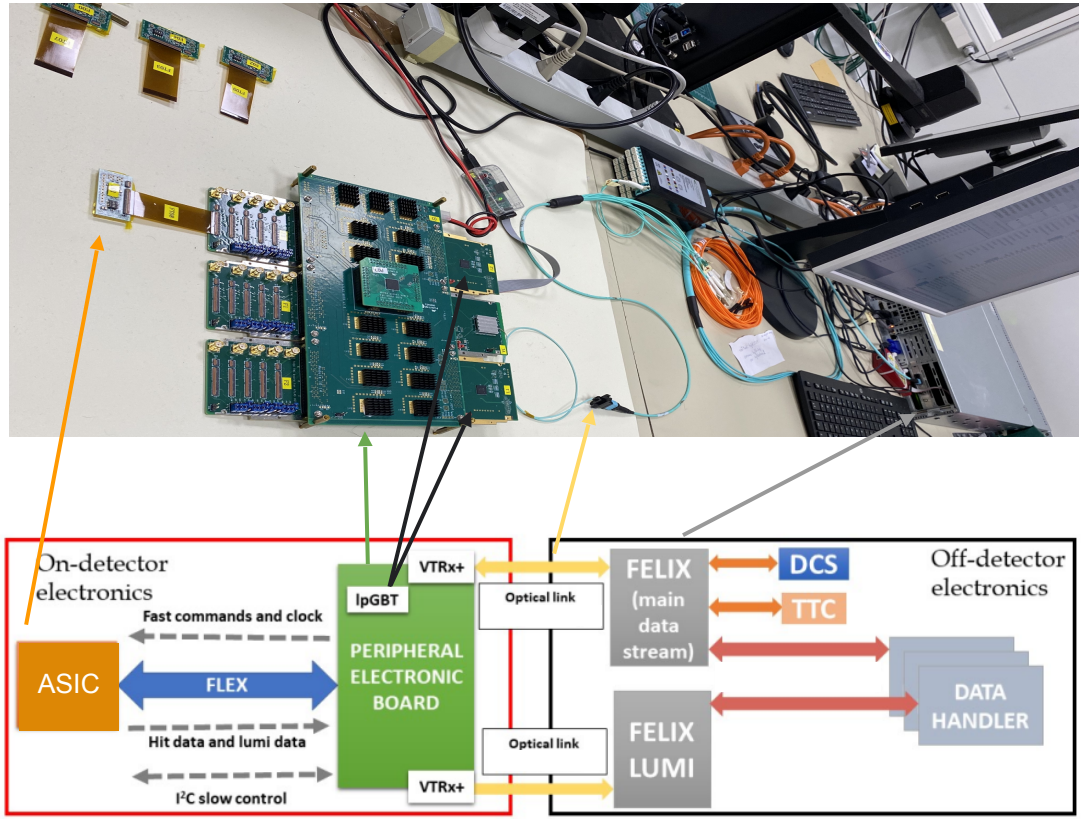
Thermal grease



HGTD : DAQ demonstrator

Goal : to develop the readout path of the detector and validate both the PEB and FELIX environment

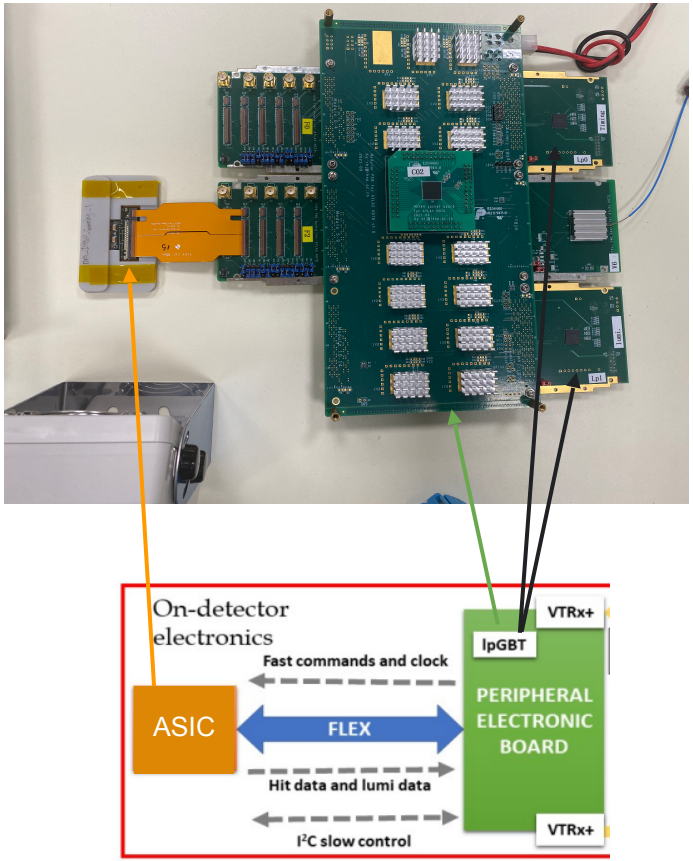
- Establish communication between the setup and FELIX
- Optimise configurations and readout ASICs
- Develop the software for timing and luminosity data acquisition



DAQ demonstrator : where do we stand ?

- Started with FPGAs that emulates ALTIROC ASIC
- Now, the readout is done with one version-2 of ALTIROC ASIC (final version to be submitted this month)
- The next step is to develop the software to configure and read the modules in parallel (16064 in total)

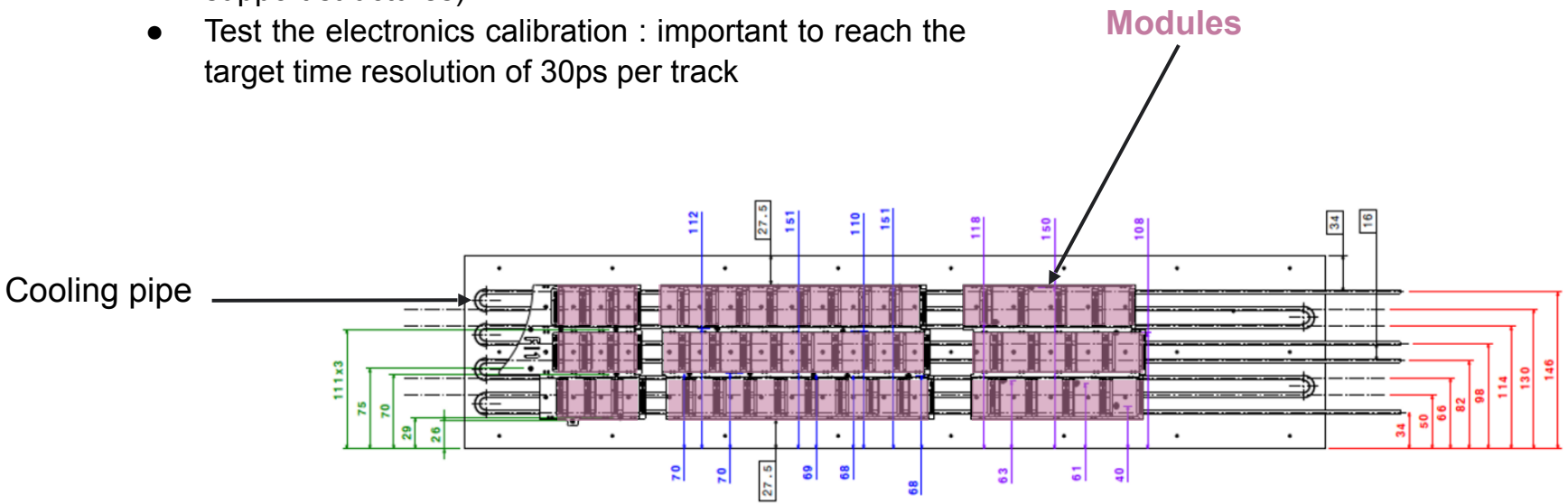
Setups in different laboratories : CERN, Nikhef, KTH (Sweden) and IHEP (China)



HGTD : Full demonstrator

Goal :

- Define the loading of hybrid modules
- Validate the full system integration (mechanical support structures)
- Test the electronics calibration : important to reach the target time resolution of 30ps per track



Summary

- The HGTD is a project for Phase-II upgrade of the ATLAS detector with the goal of removing pileup and providing precise time measurements
- This will enhance the performance of physics object reconstruction and so increase the physics potential for the HL-LHC phase

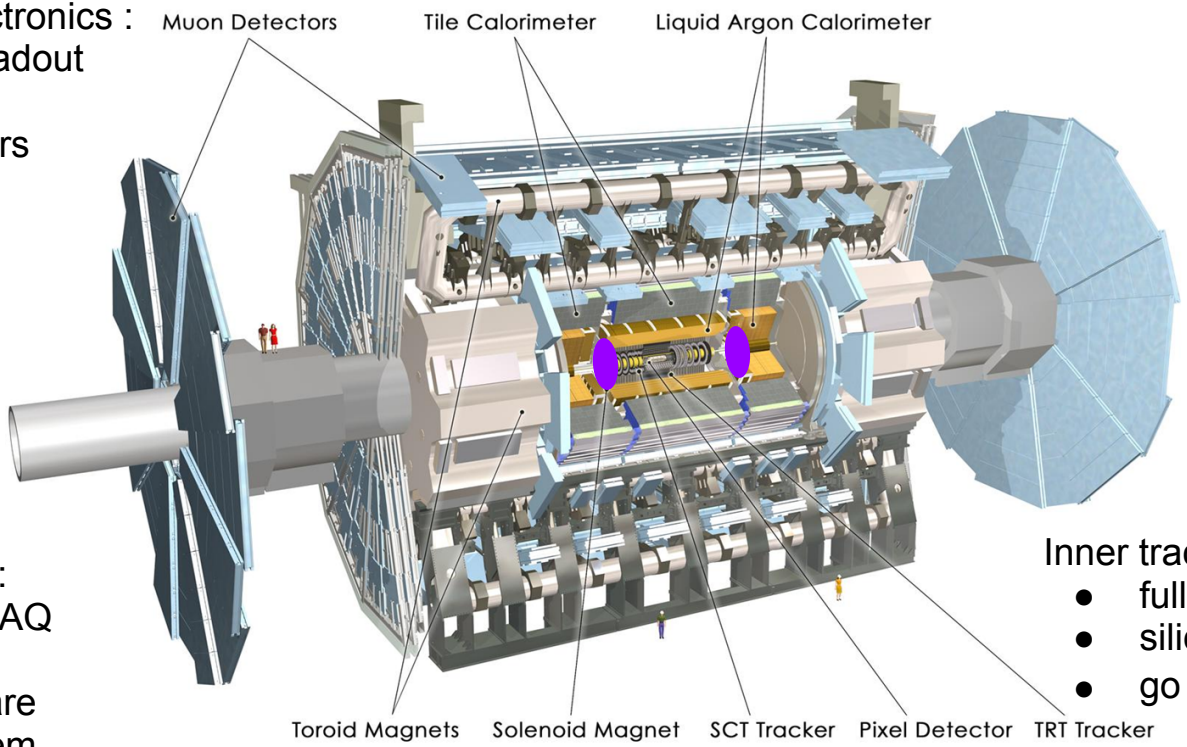
- The demonstrators are crucial to test and validate the design of the detector
    - Heater demonstrator : validate the structure design and develop the cooling
    - DAQ demonstrator : develop the readout chain
    - Next step : full demonstrator to validate the full system integration

Thank you for your attention

ATLAS : Phase II upgrade

Muon detector :
- upgrade electronics : front-end, readout and trigger
- new chambers

Calorimeter :
- upgrade electronics : new front-end and readout



HGTD :
- new detector

Trigger and DAQ :
- upgrade TDAQ systems
- new hardware trigger system

Inner tracker :
- full replacement
- silicon-only design
- go from $|\eta| < 2.5$ to $|\eta| < 4$

HGTD : Hybrid Module