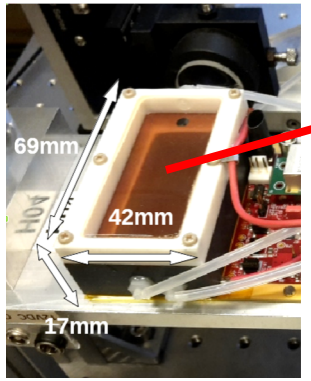
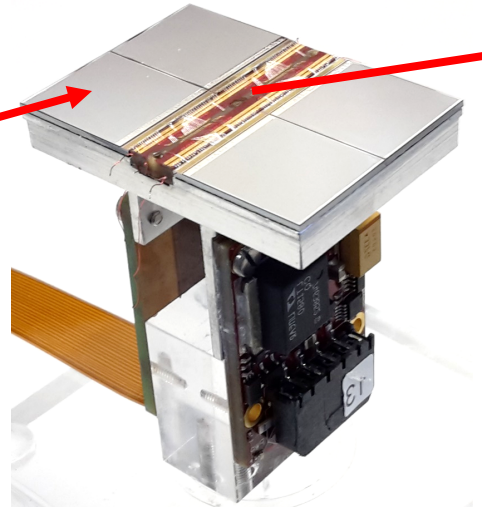
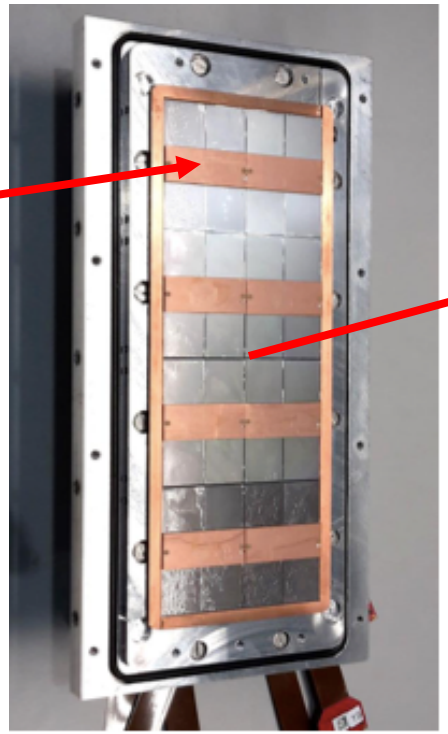
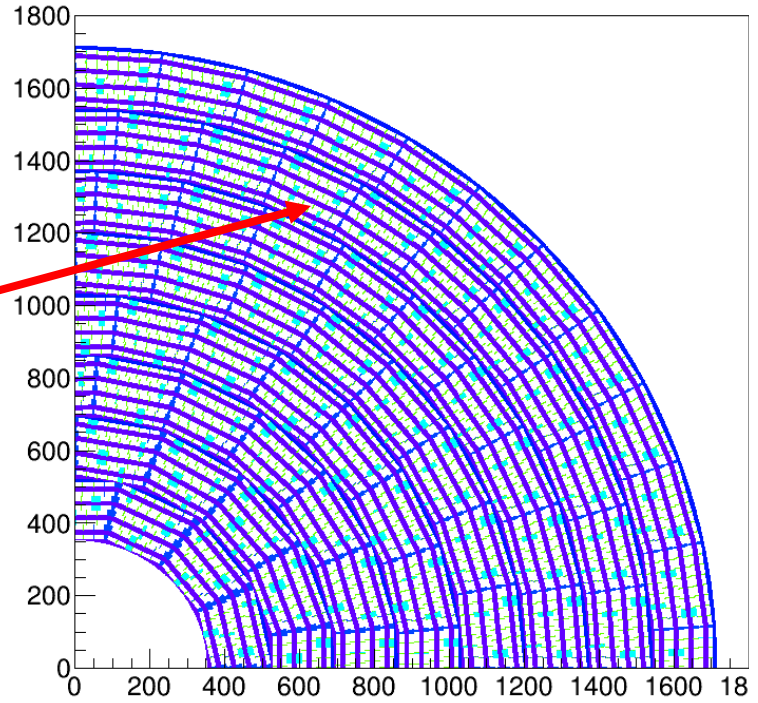
Pixel TPC









Single chip 2017

Quad 2018

Module 2019

TPC plane

Equalisation of the 8-quad module

With the two concentrators we can read out maximally 32 chips.
In the concentrator special software is running.
The procedures to configure and read out the individual chips needed to be revisited.

There are three modes of operation that are relevant for the operation of the module:

-A data taking by injecting testpulses and analysing these data
-B the equalisation procedure (see details further on)
-C data taking
    1. noise data;
    2. with a laser beam and trigger (time stamp)
    3. testbeam data with a trigger and a silicon telescope (e.g. in a magnetic field)

We can reliably take data in mode A: with the full detector injecting testpulses.

Equalisation of the 8-quad module

The equalisation procedure has the following steps.
The chips are put in a special data taking mode where the thresholds are written to the data stream and the per pixel the number of hits is counted.

Several threshold scans are performed to measure the noise level per pixel. Data is taken by selecting colums and rows with a spacing of 4 or 8. The rest of the pixels are masked.
Two threshold scans are performed for the trim values of 0 and 15.

For this data sets the DAC trim values are calculated thus that a common threshold can be used for all the pixels. This is called equalisation.

Finally a threshold scan – after equalisation - is performed using the DAC trim values per pixel. If this is all succesfull, the DAC trim values can be used for data taking.

Equalisation of the 8-quad module

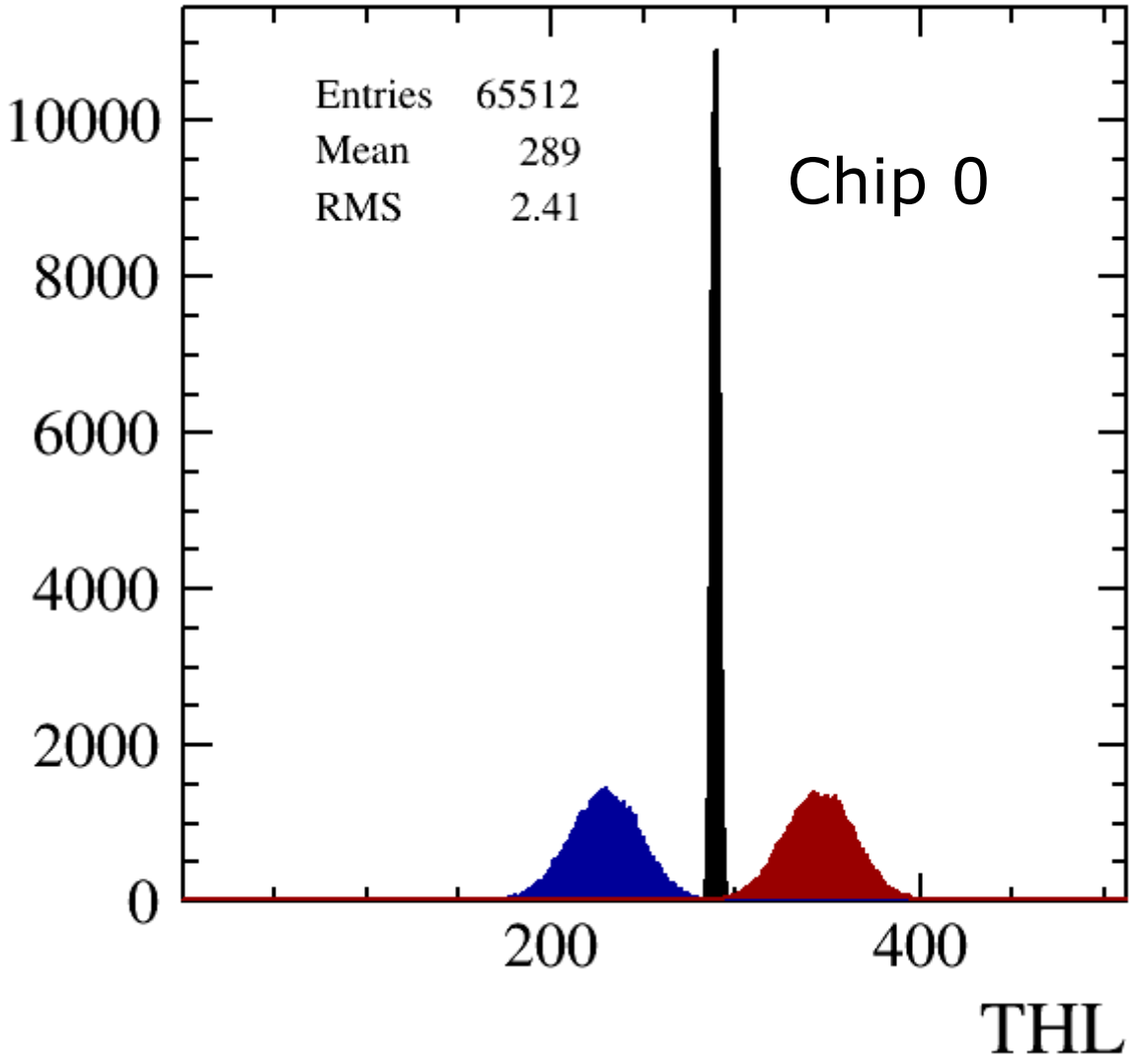
Here the results for spacing 4 for all the chips that can be read out.
In total 28 chips; chips 7, 24, 25, 31 have a problem

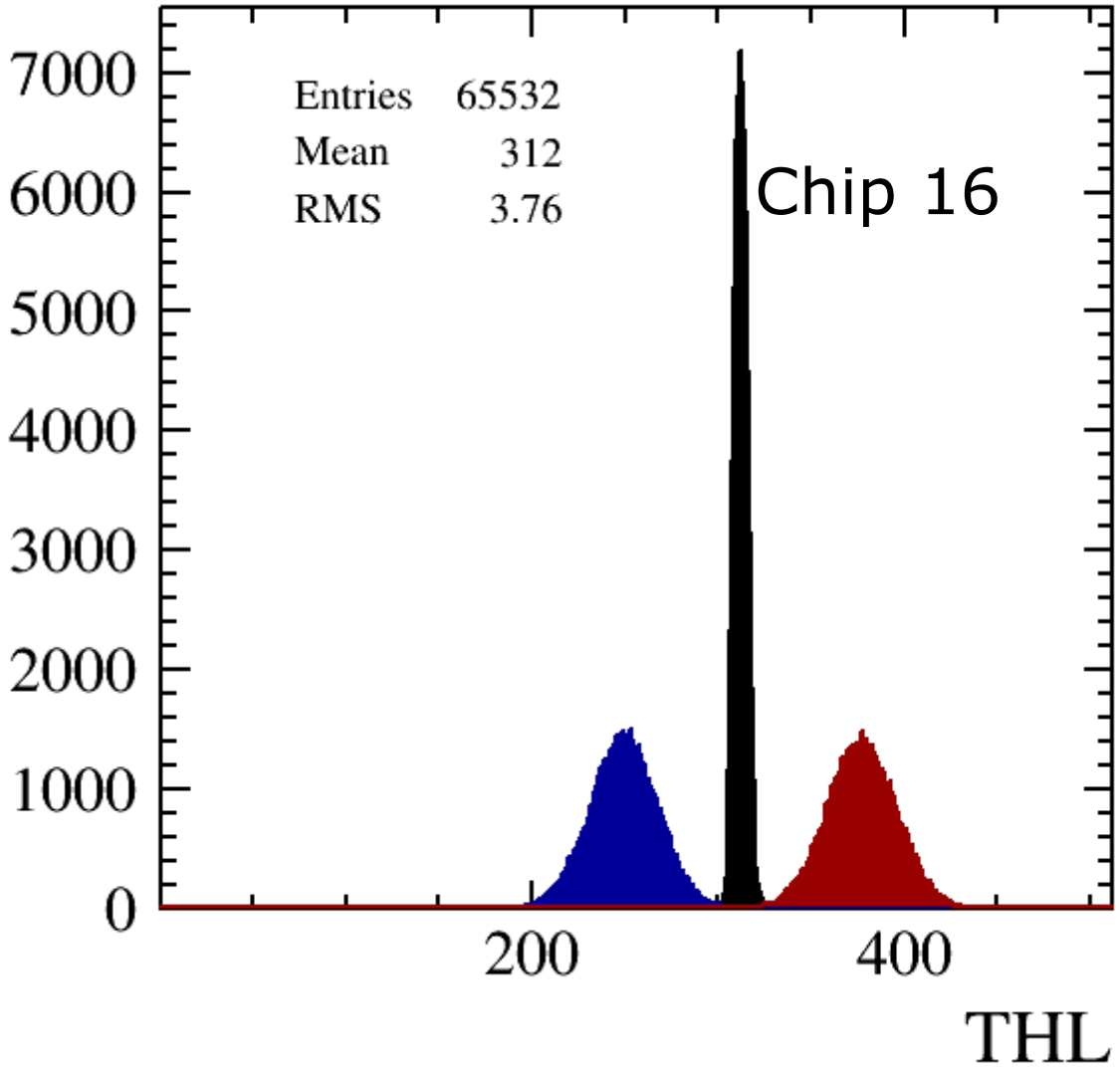
Note] number of active links : 2
[Note] dev 0: W0030_C08 (1e83) mapped to chip nr 9
[Note] dev 1: W0030_C09 (1e93) mapped to chip nr 10
[Note] dev 2: W0030_K05 (1e5b) mapped to chip nr 11
[Note] dev 3: W0023_E09 (1795) mapped to chip nr 12
[Note] dev 4: W0023_D08 (1784) mapped to chip nr 13
[Note] dev 5: W0023_E08 (1785) mapped to chip nr 14
[Note] dev 6: W0023_H08 (1788) mapped to chip nr 15
[Note] dev 7: W0030_F06 (1e66) mapped to chip nr 0
[Note] dev 8: W0030_E07 (1e75) mapped to chip nr 1
[Note] dev 9: W0030_F07 (1e76) mapped to chip nr 2
[Note] dev 10: W0030_M05 (1e5d) mapped to chip nr 3
[Note] dev 11: W0023_H09 (1798) mapped to chip nr 4
[Note] dev 12: W0023_I09 (1799) mapped to chip nr 5
[Note] dev 13: W0023_I06 (1769) mapped to chip nr 6
[Note] dev 14: W0030_C07 (1e73) mapped to chip nr 8
[Note] dev 16: W0030_I04 (1e49) mapped to chip nr 1
[Note] dev 17: W0030_A05 (1e51) mapped to chip nr 2
[Note] dev 18: W0030_H02 (1e28) mapped to chip nr 3
[Note] dev 19: W0023_E04 (1745) mapped to chip nr 4
[Note] dev 20: W0023_F04 (1746) mapped to chip nr 5
[Note] dev 21: W0023_G04 (1747) mapped to chip nr 6
[Note] dev 22: W0023_H03 (1738) mapped to chip nr 7
[Note] dev 23: W0023_E05 (1755) mapped to chip nr 10
[Note] dev 24: W0023_H04 (1748) mapped to chip nr 11
[Note] dev 25: W0023_D06 (1764) mapped to chip nr 12
[Note] dev 26: W0023_H06 (1768) mapped to chip nr 13
[Note] dev 27: W0023_J06 (176a) mapped to chip nr 14
[Note] dev 28: W0030_G03 (1e37) mapped to chip nr 0
[Note] 28 active devices

In black concentrator 0 chip 0-15

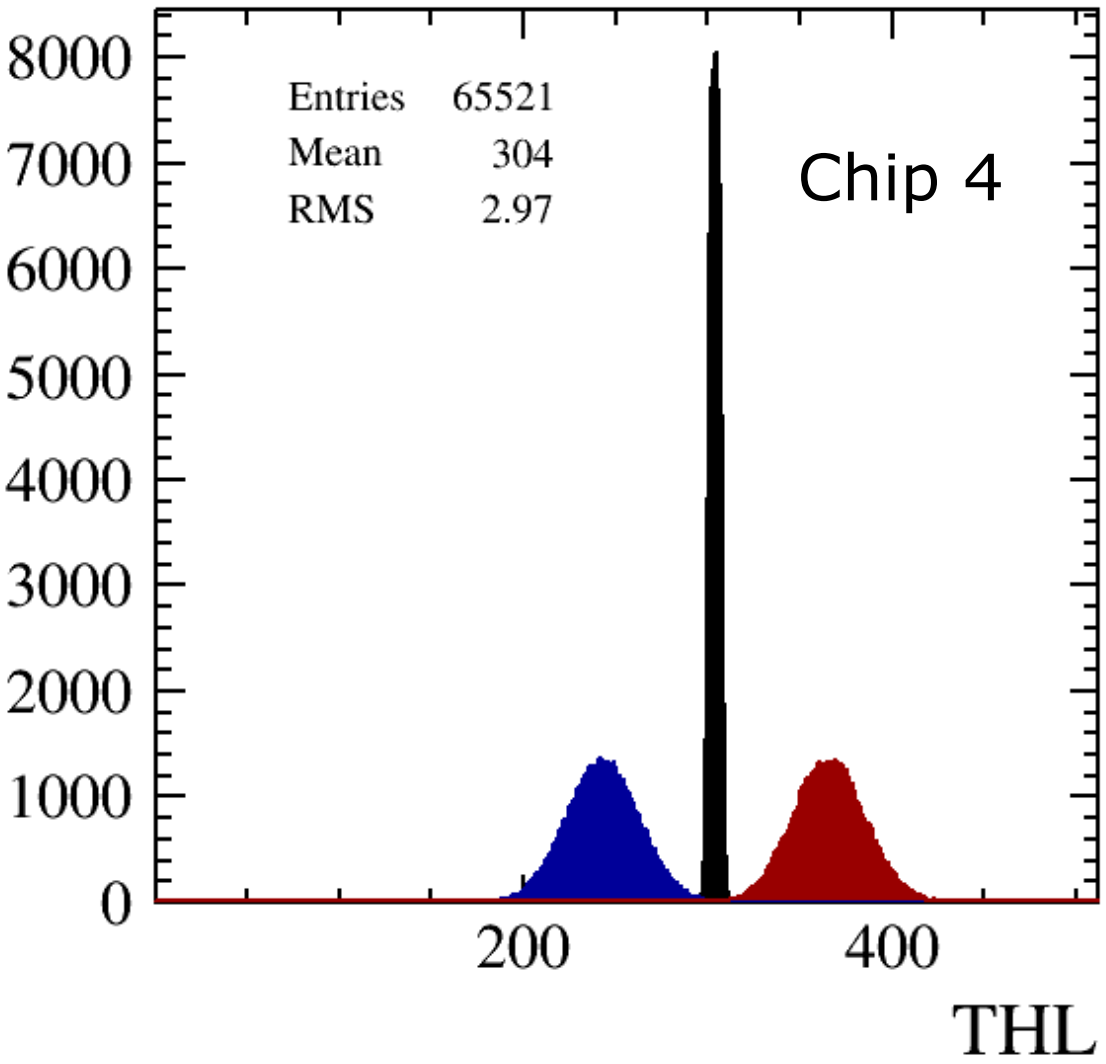
In blue concentrator 1 chip 16-32

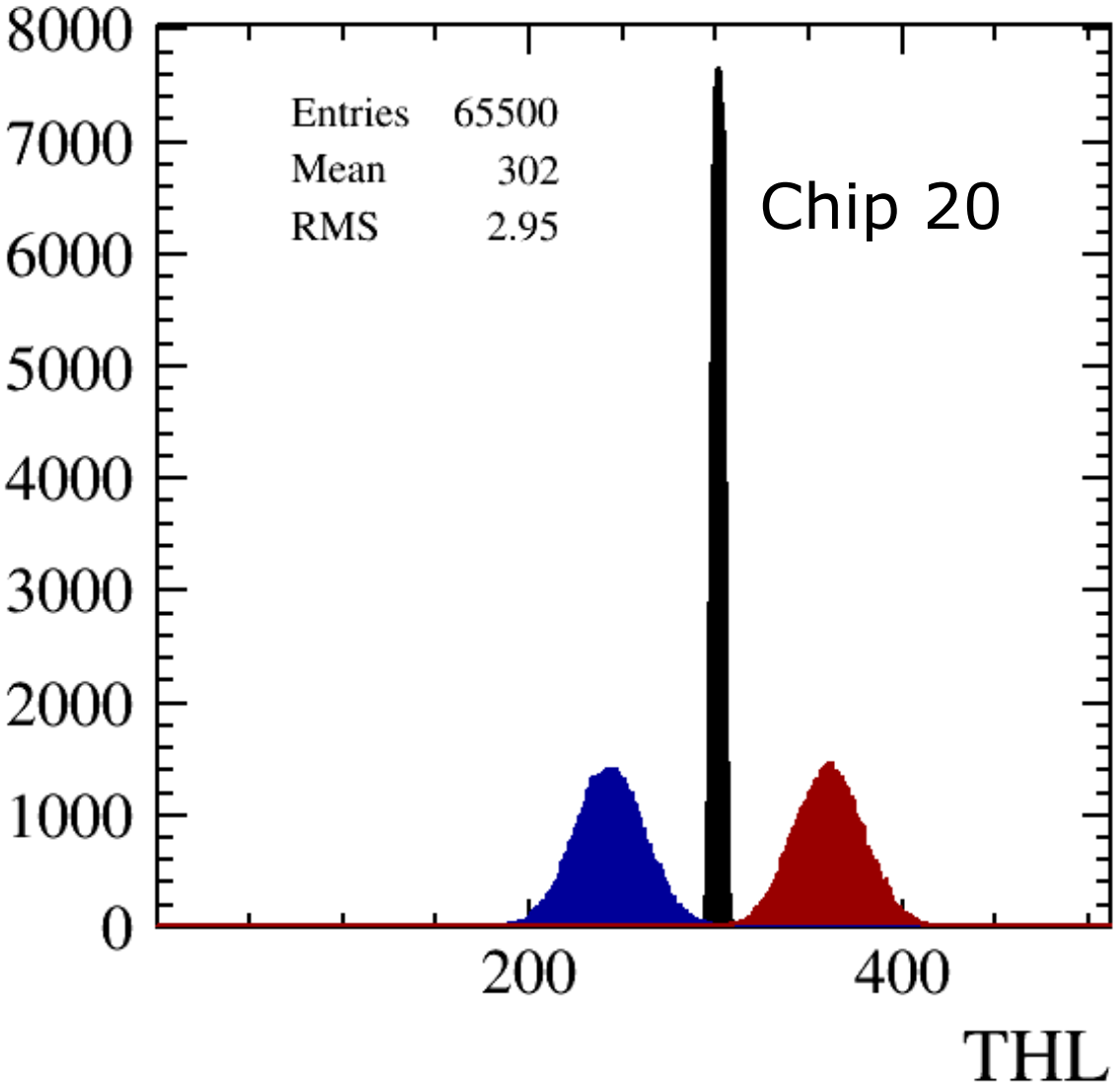
Equalisation of the 8-quad module



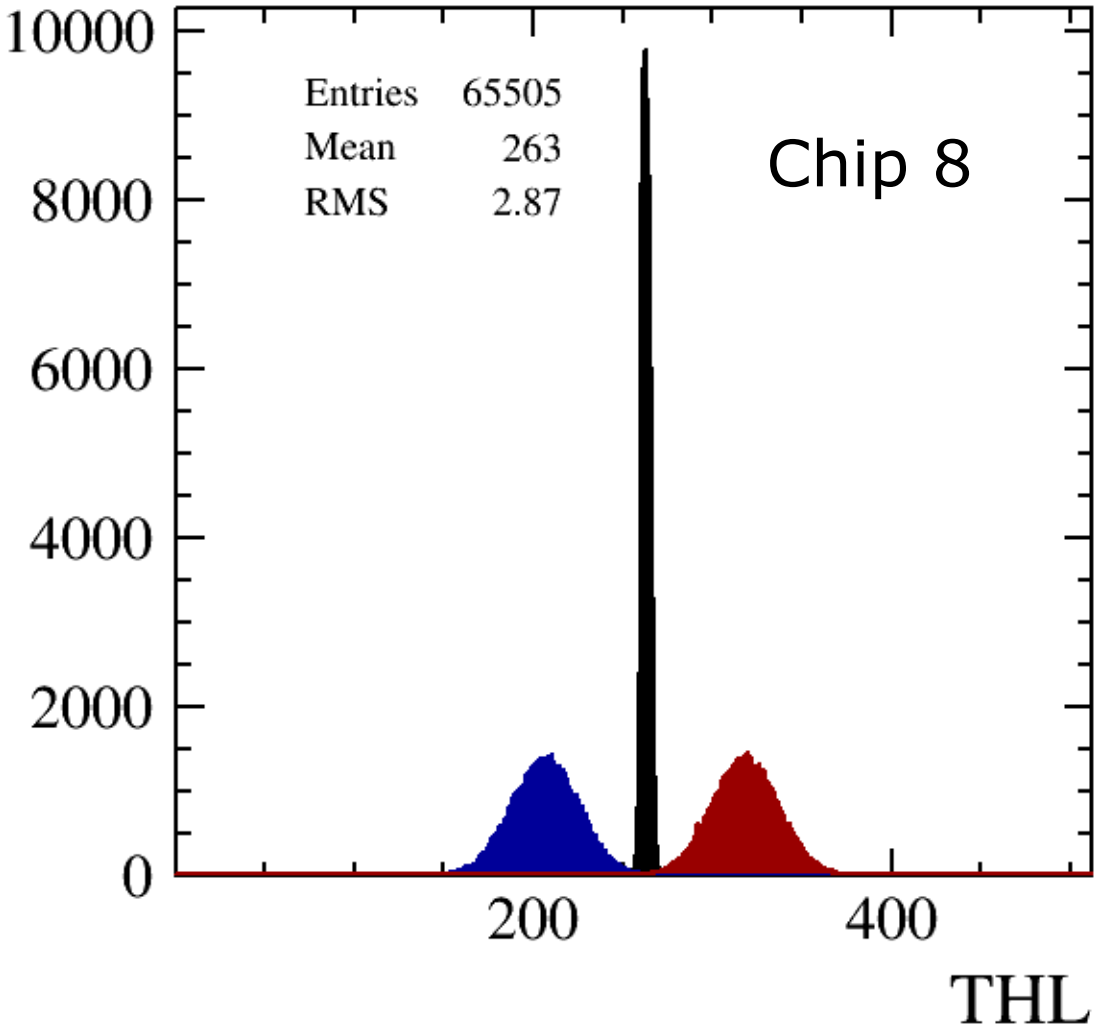


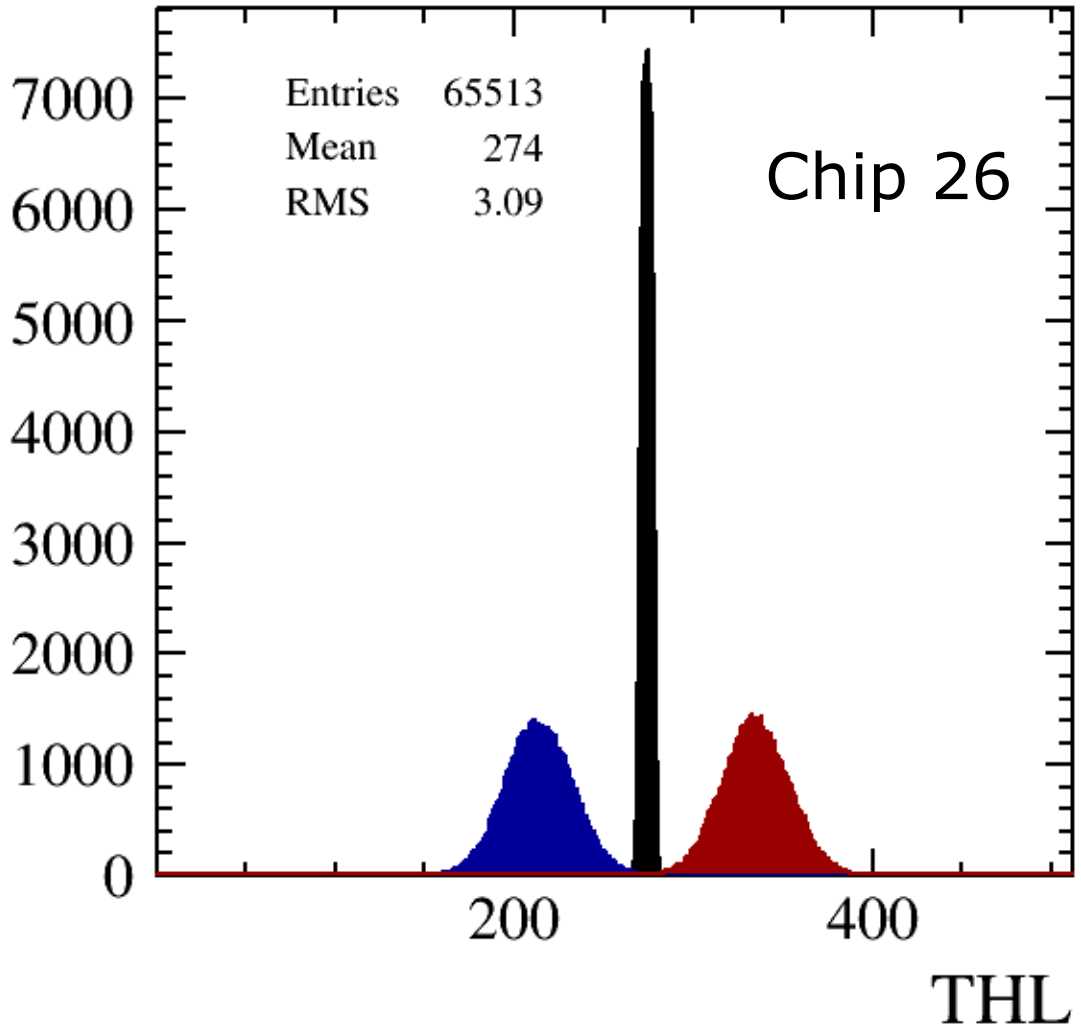
Equalisation of the 8-quad module



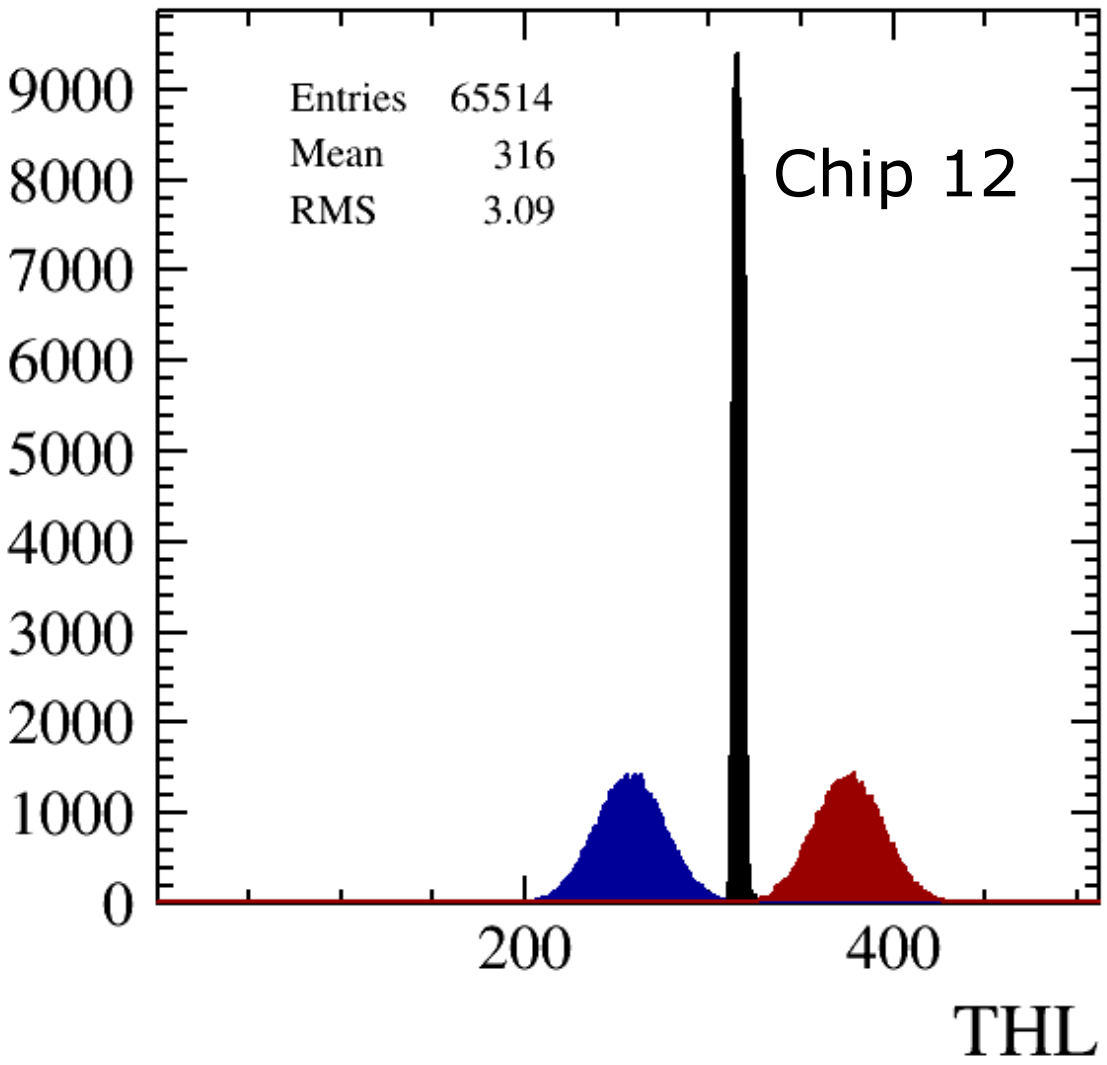


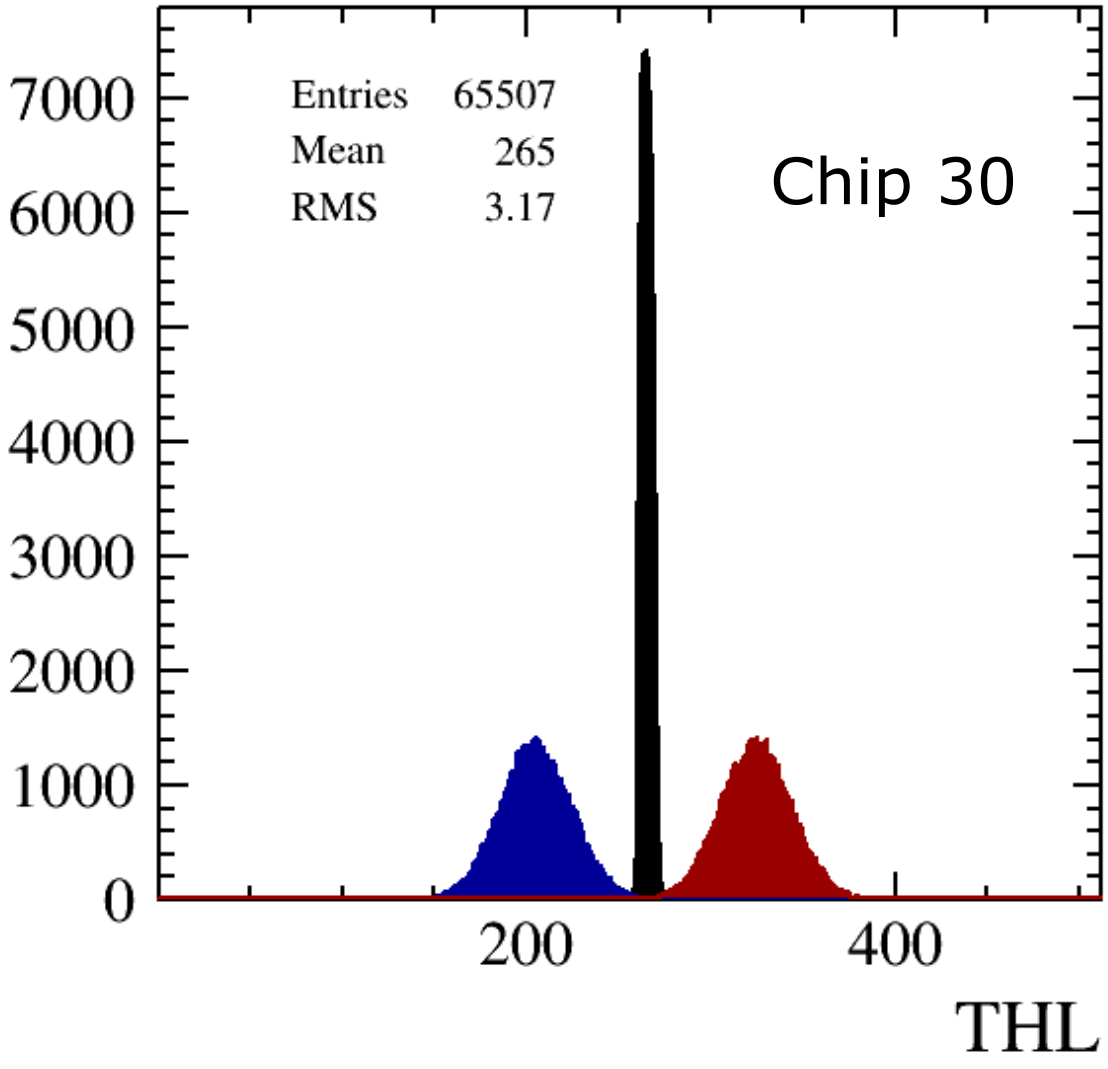
Equalisation of the 8-quad module





Equalisation of the 8-quad module





Equalisation results

The mean threshold per chip varies between 263 – 319 counts.
The rms of the equalized chip varies between 2.8-3.7 counts.

The average rms of the noise distribution per pixel is 7.5 counts.
It is similar for all chips.

Conclusions

Thanks to the efforts of may of us and in particular the ET experts Sander van Doesburg, Henk Boterenbrood, Bas van der Heijden and the support of the Ruud Kluit and Martin van Beusekom, we can now run the daq and in a few hours equalize all the chips.

However, we are not yet where we want to be…

The next steps ahead are (in order):
- taking noise data and the masking of noisy pixels
- taking laser track data and fully test the quad module and measure its performance

The cherry on the cake is data taking at a test facility like DESY. Due to COVID we had to re-arrange our testbeam plan. But we will get there.