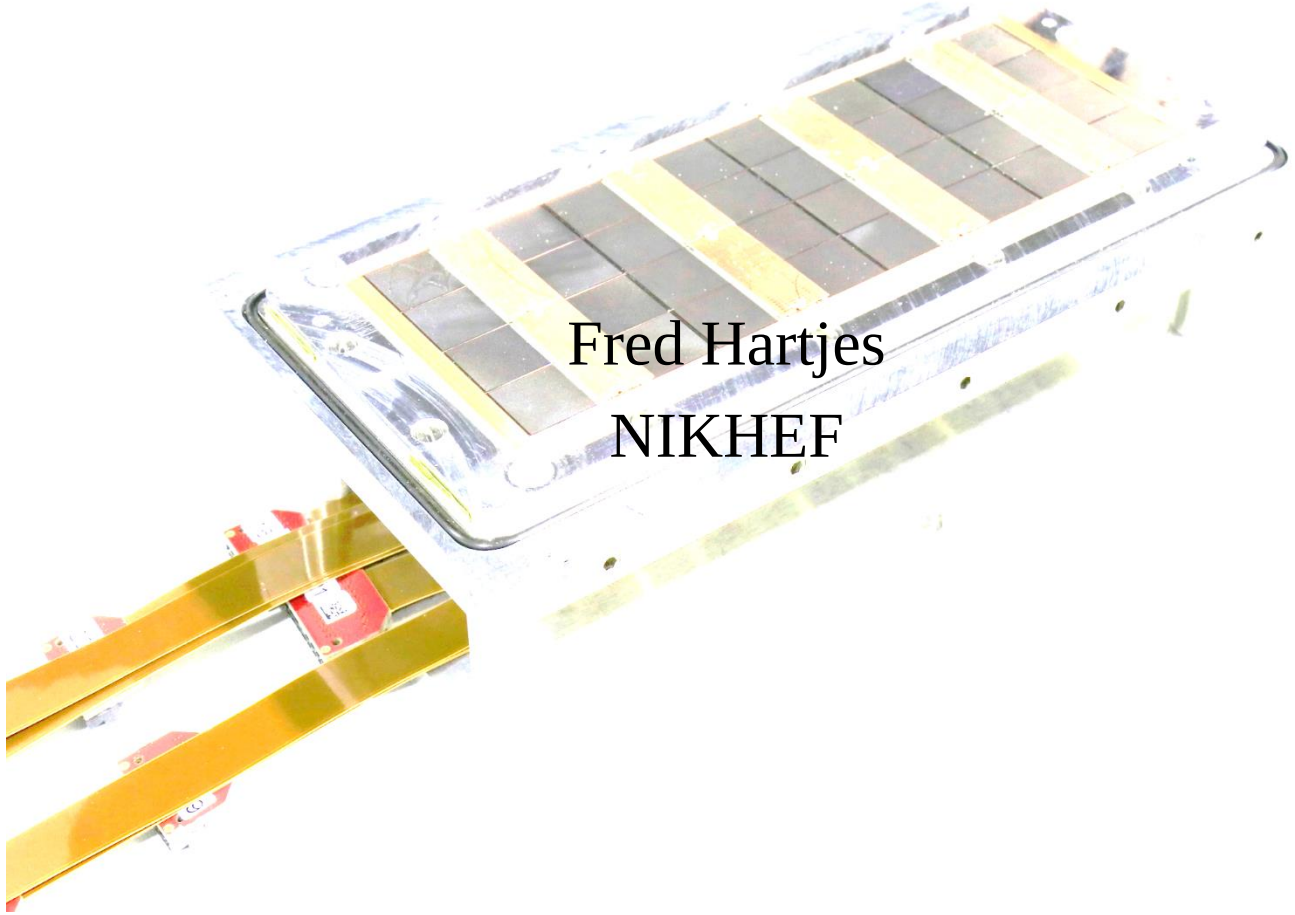
Using TimePix4 for a new gaseous detector unit



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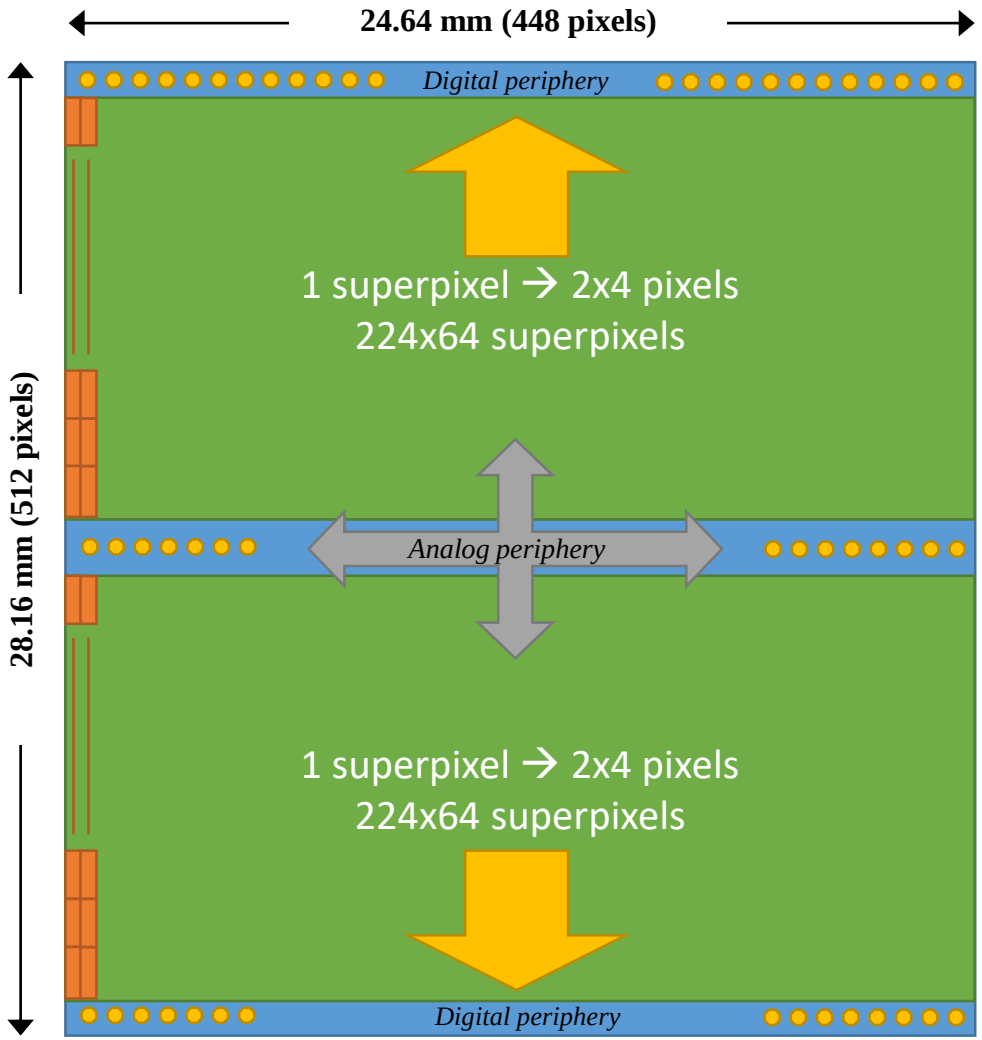
TimePix4 layout

- 512 x 448 pixels
- Cell size 55 x 55 μm (on external surface)
  - 55 x 51.875 (internal)
- External pads also cover analog and digital periphery
- Using Through Silicon Via (TSV) connections multiple chips can be joined without any dead space (in case of silicon detectors)
- Die dimensions 28.215 x 24.695 mm (TSV)

- For using wire bonds the die has to be extended on both sides by 0.9 mm
- Not all IO or supply pads on both sides need to be connected
  - Only output lines are crucial



TPX4 layout without bonding pads

TimePix3 vs TimePix4

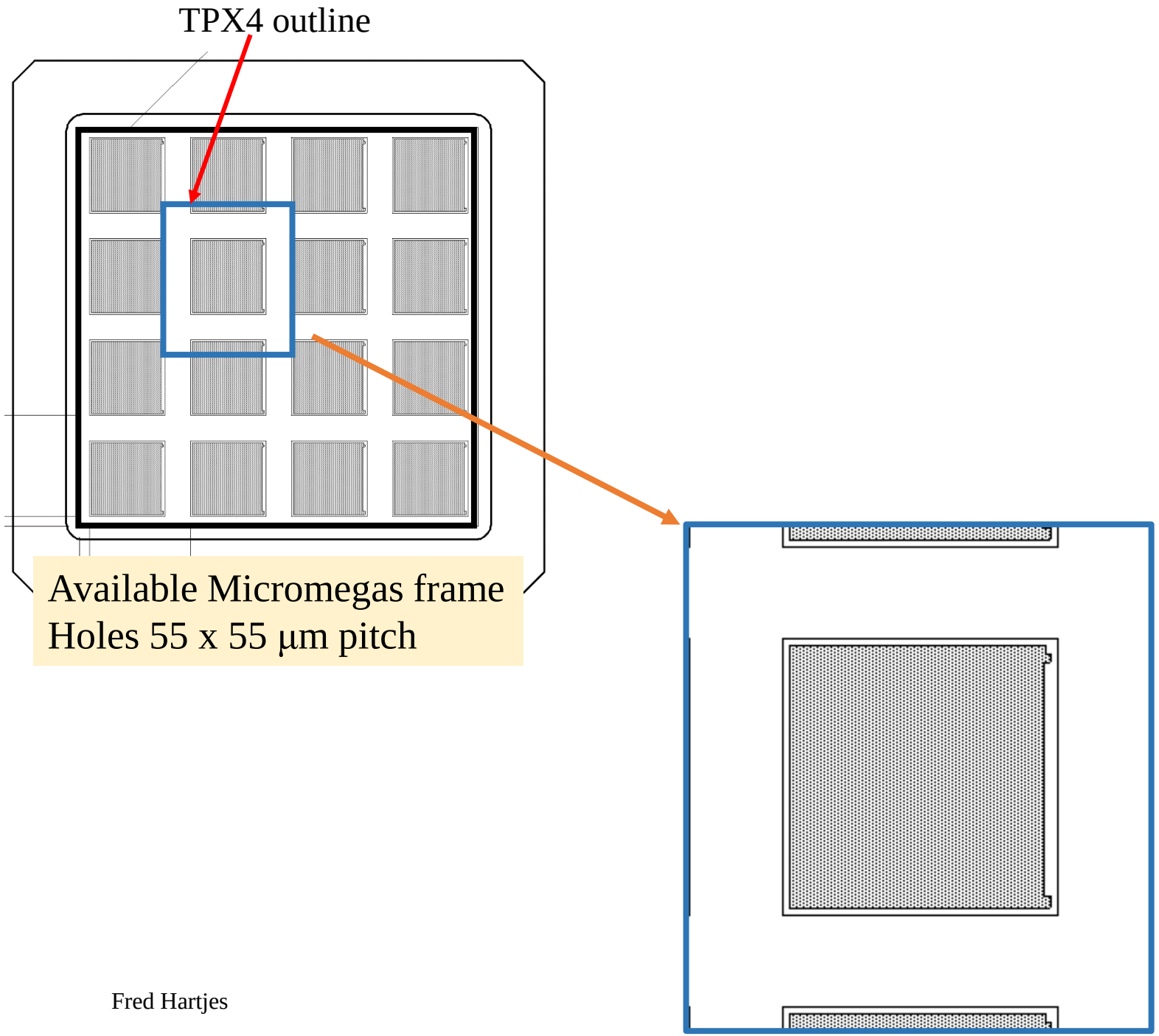
	TimePix3	TimePix4
# of wire bond pads	110 (92 used)	147 (~ 100 will be used)
Pixel pitch (µm)	55 x 55	55 x 55
Wire bond pitch µm)	73 (signals) /146 (power)	165
Minimum threshold	500 e^-	500 e^-
LV power (digital + analog)	1.5 V	1.2 V
Active surface (mm^2)	198	694 (3.5 x TPX3)
RO rate per unit of active surface	< 43 Mhits/cm^2/s	357.6 Mhits/cm^2/s

Initial TPX4 testing

- First chips are being electronically tested at Nikhef (ET)

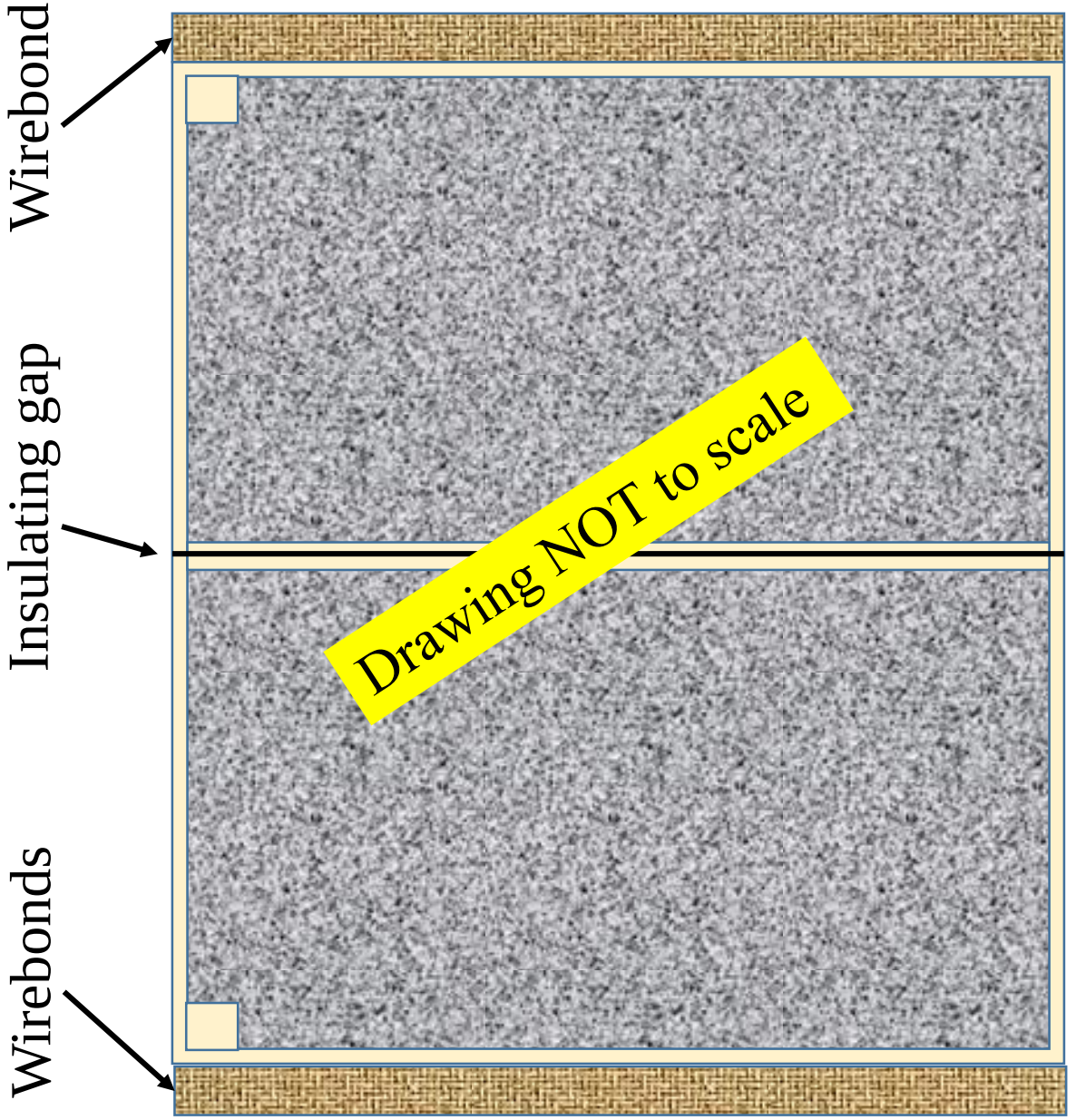
- Using a loose Micromegas we may produce ‘physical’ signals from gas avalanches
- Initially without protection layer
  - Low gain using a He mixture

- Lateron adding a protection layer on a single chip
  - Yevgen in Twente?
  - => testing without risk at larger signals



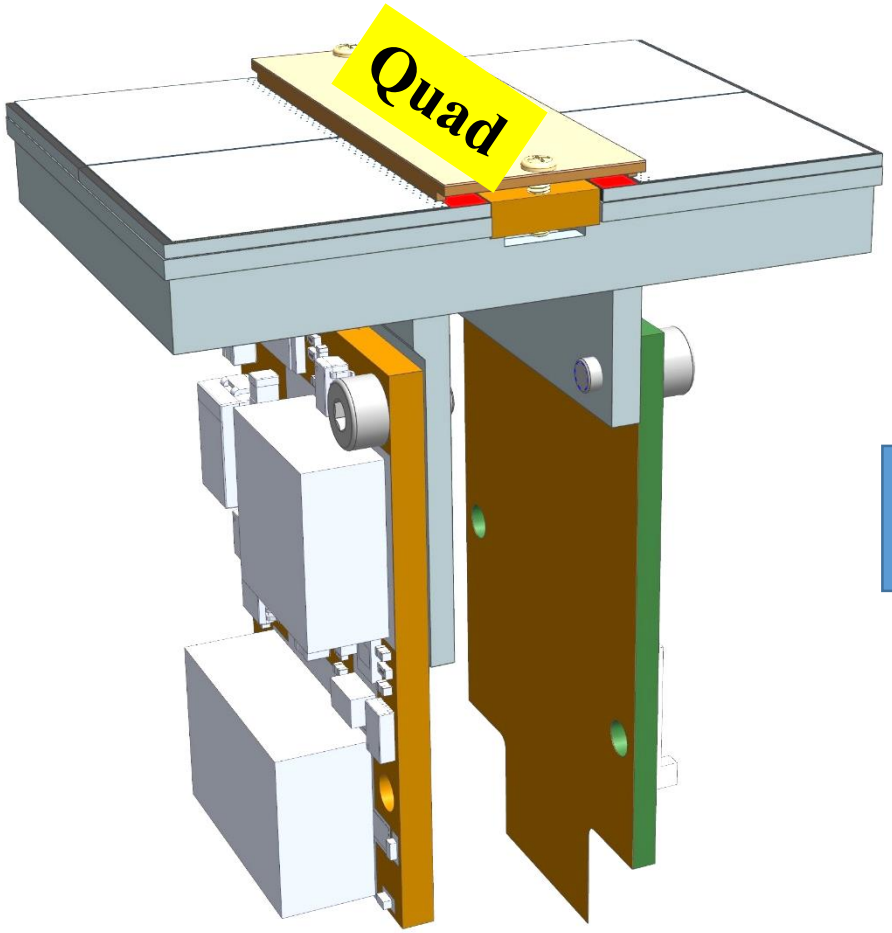
Next step: adding InGrid

- Total active surface: **694** mm^2
- Add surrounding dyke of 165 μm wide
- Divide the grid into two by a central dyke 220 μm wide to reduce the grid capacity
  - => less risk on discharge damage
  - Not sure if really needed, but we may start with a safe approach
- Add two 1 mm^2 pads for grid voltage connection
- Final active surface using InGrid: **669** mm^2
- => we loose **3.6%**
- **Note: wafer size 12”**

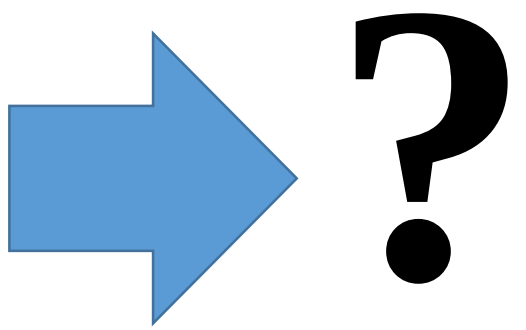


How to design a detector unit based on TPX4

- **New start from scratch**
- But using the experience with the present quad
- TPX4 has 3.5 bigger detection surface
- => We may replace the four TPX3 chips by a single TPX4
- Making detector units with two or more TPX4 chips has no advantage
  - More complex wirebond PCB
  - Always one LV PS per chip needed
  - For ILD: large unit => more dead space on a module
  - Assembly more critical (risk on damaging the grids)
    - => lower yield



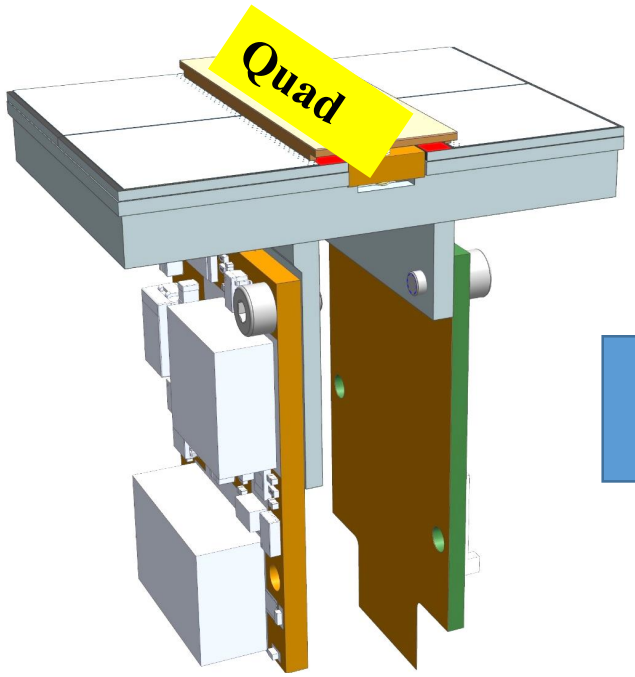
Design based on TPX3



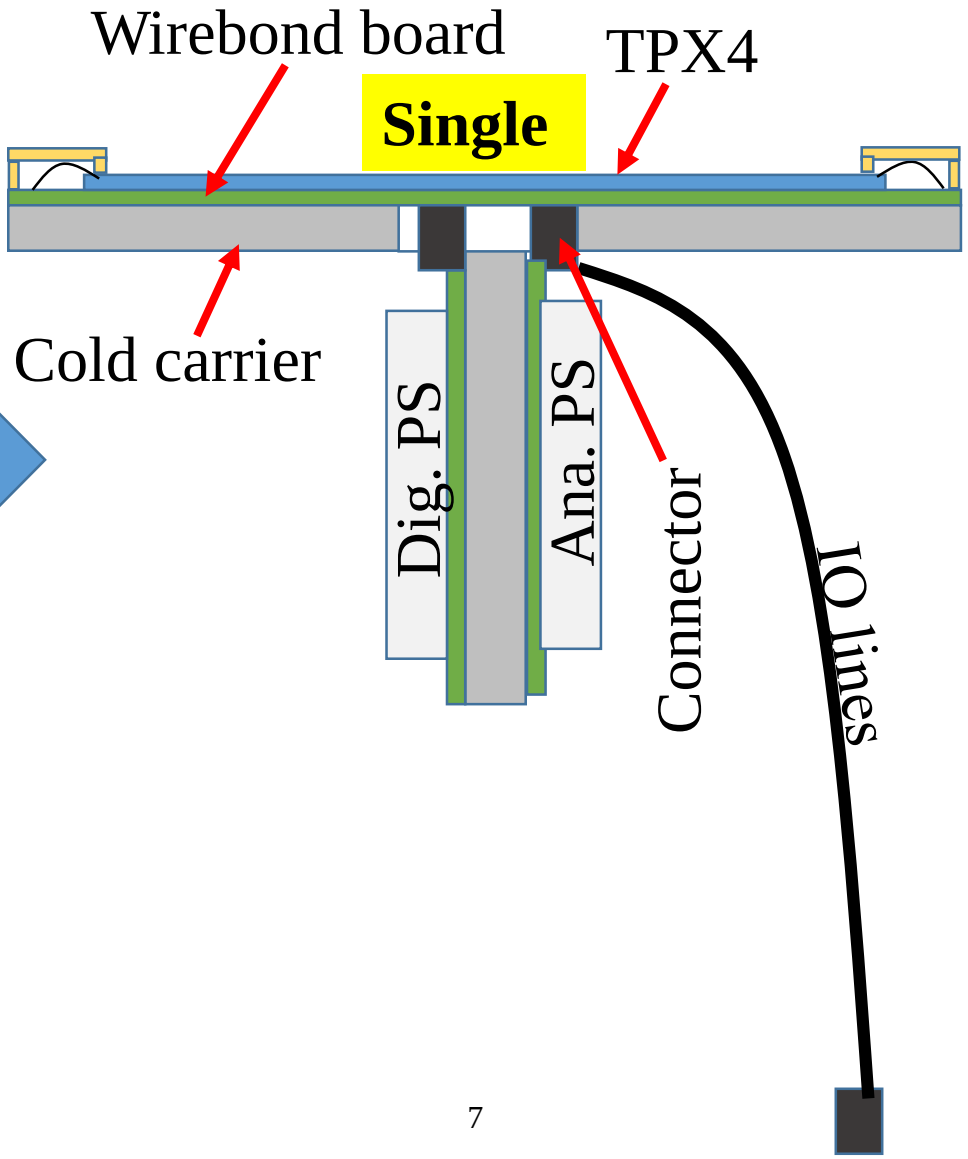
?

Design principles ‘Single’ using TPX4 (wirebond version)

- **Not using integrated flexes**
  - Nuisance during assembly
  - Makes PCB more expensive
- TPX4 attached to a wirebond board
  - Board has multitude of vias for better heat conductivity
- Wirebond board provides good thermal contact between TPX4 and the ‘cold carrier’



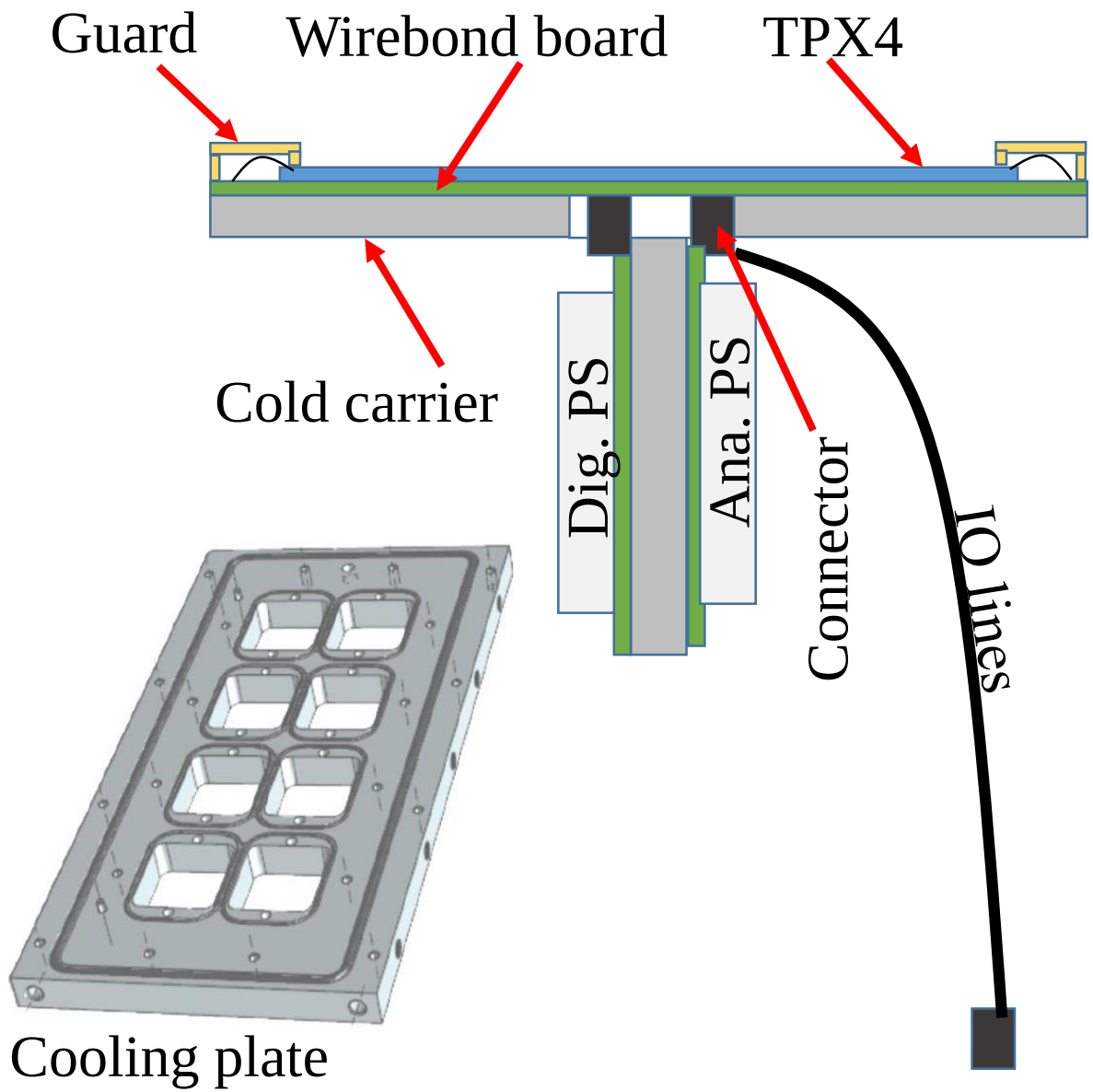
Design based on TPX3



Concept of ‘Single’

- Cold carrier mounted on a cooling plate
- 3 connectors on back of wirebond board

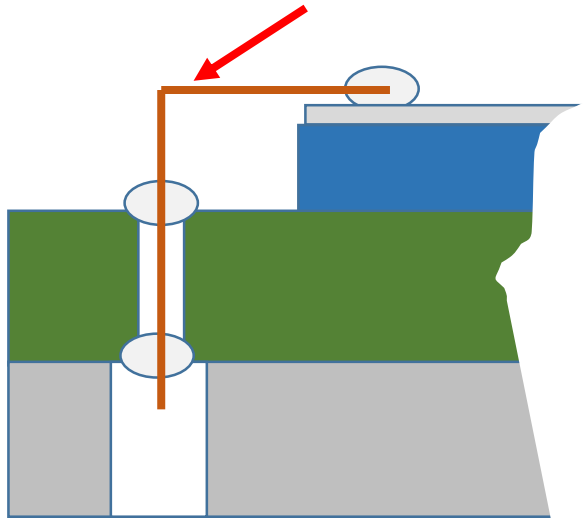
1. To a LV voltage PCB on a cooling plate
   - Has to make thermal contact to the cooling plate
   - Give analog and digital PS their own LV PCB?
2. To a 3-pole HV connector
   - Filtered connection to grids/guards on back wirebond board
3. To the IO lines
   - Using separate flex



Connecting grid voltage

- For the present quad very time consuming and enervating
- Grid voltage connection on the edge of the wirebond board
  - 80 μm insulated wire
  - Soldered to plated hole on wirebond PCB
  - Silverglued onto the grid of the TPX4
- Wirebonds are not reliable
  - Bad attachment on InGrid
- Problem: how to cope with manufacturer's HV rules on a PCB
  - Rules require distances like 5 mm for insulation of the grid voltage
  - But we applied successfully on an InGrid an insulation distance (pillars) of 50 μm
  - My guess: for our application we may easily reduce the insulation distance to < 1 mm
    - We handle the PCBs as delicate items
    - Used in low humidity environment, tight temperature range

Insulated wire



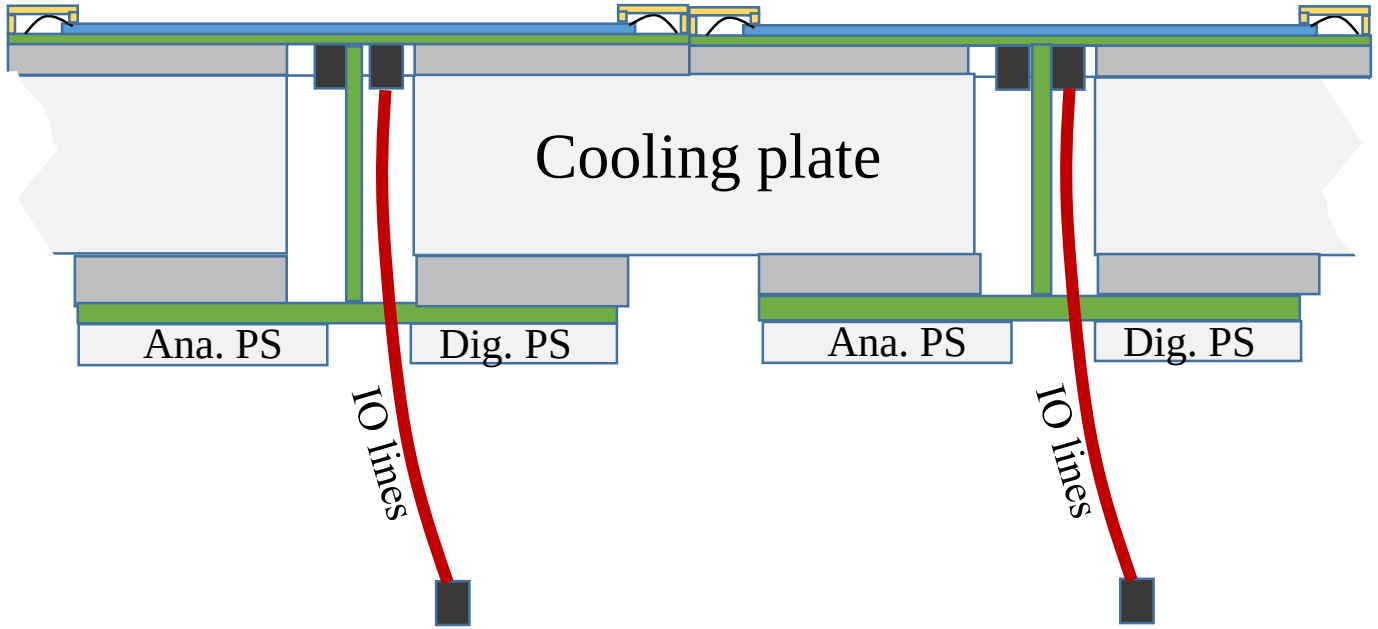
Total ‘Single’ dimensions and active surface

- On each side (top and bottom)
  - 0.9 mm wirebond extension
  - 3.5 mm for wirebond PCB (estimated)
- **Length** 29.96 + 2 x 3 ≈ **36.0 mm**
- **Width 24.695 mm**
- (Present quad: 39.6 x 28.38 mm)

- => total ‘Single’ detector surface 889 mm^2
- Available area for ionization detection 669 mm^2
- => 669/889 = **75.2% of total surface**
  - For quad 68.9%
- But using **TSV 89% of total surface**
  - Reserving 2 x 0.2 mm for grid/guard HV wires

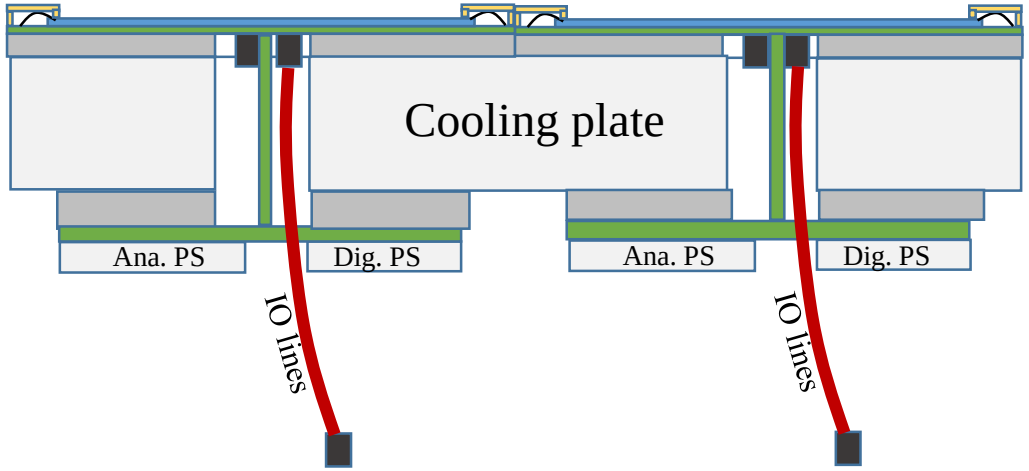
Alternative assembly showing two Singles

- We are free of choosing another orientation for the LV PCBs
  - Separate them from the wirebond board and cold carrier
  - Mount them onto the backside of the cooling plate
- Advantage
  - Detector existing of TPX4, WB PCB and cold carrier, is much less risky to handle during assembly
  - The detector plane will be less deep



Conclusions and prospects

- Using the “Single” as a gaseous pixel detector has many advantages over the present Quad
  - Larger seamless detection surface
  - Easier assembly
  - Larger pitch of wirebond pads, less wirebonds
- Using detector units of a single TPX4 may be the most advantageous solution
- Using the experience gathered while designing and assembling the present Quad, the ‘Single’ will have a much less laborious assembly
  - Quad requires about 2 days for one person
  - Single may need about 0.5 day



- **Like for the Quad, the design of the Single is mostly ruled by the mechanical design of the electronics**
- **The actual design can only be made in close collaboration with the PCB designers**