Gating grid tryout to reduce ion backflow

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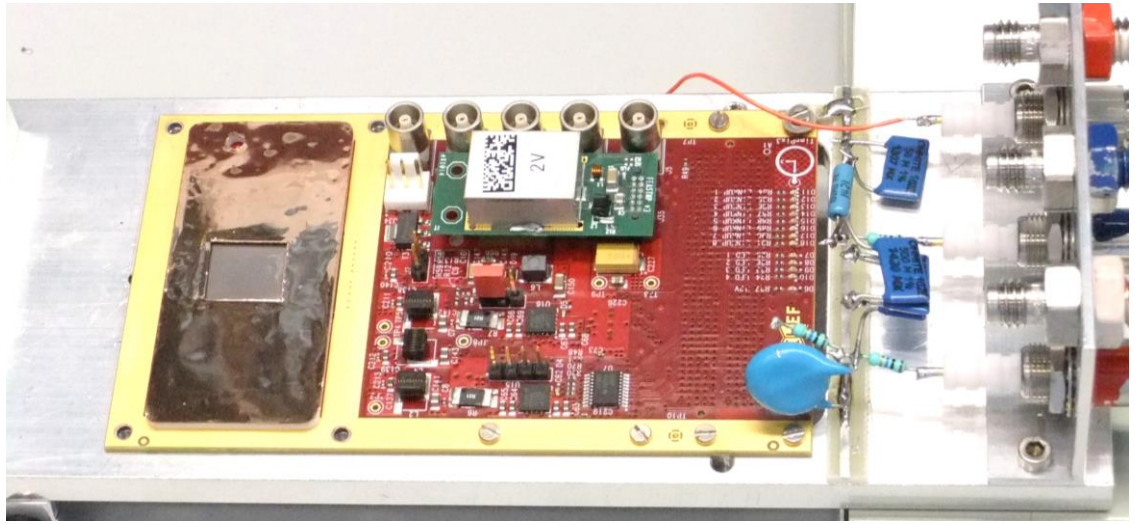
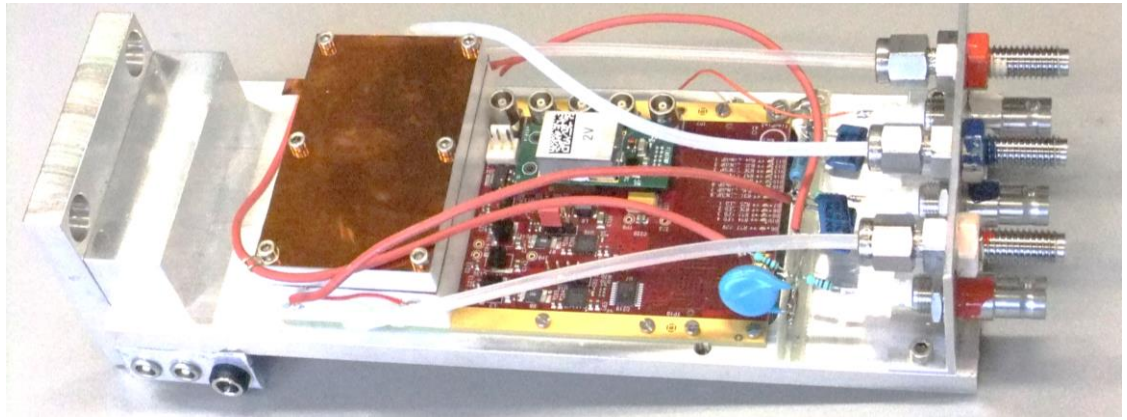
Nikhef/Bonn LepCol meeting
April 6, 2020

Test setup of the gating grid

- Peter's suggested distance to the primary grid is very small (250 μm)
- => we cannot put such a grid on an existing quad or in the 8-quad testbox without damaging the existing grids



- For a tryout we may best use an existing TPX3 chip board (from the 2017 testbeam in Bonn) with a bare TPX3 chip on it
  - Equipped with a laser window
  - Drift distance 15 mm

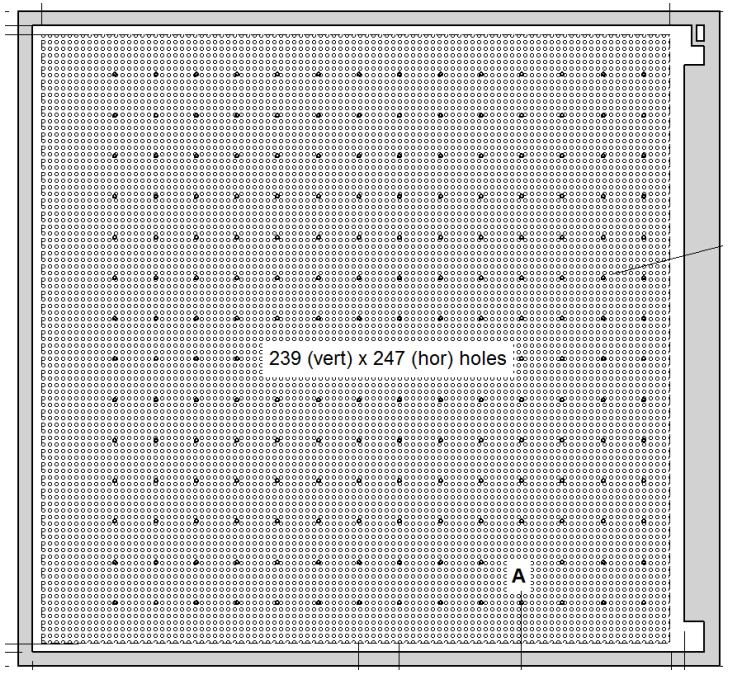


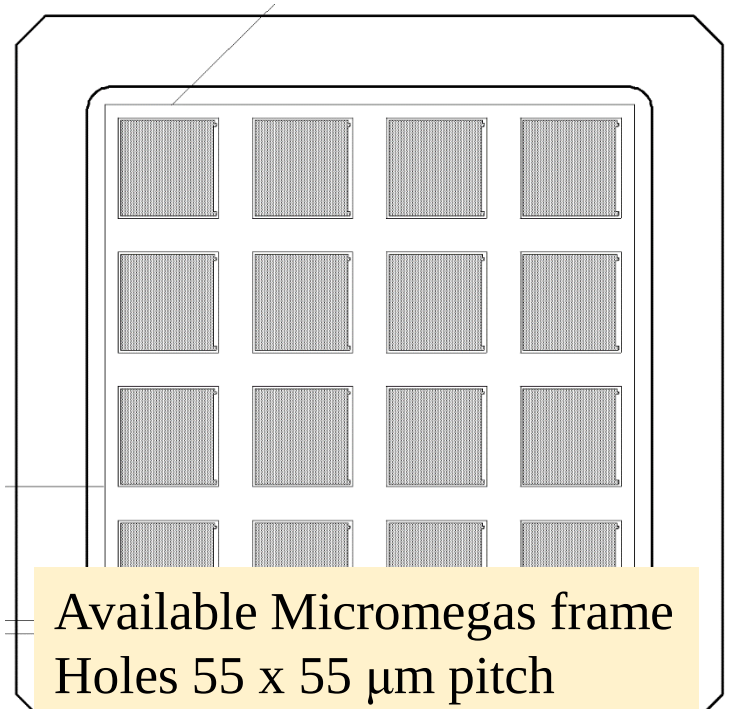
Assembling the gating grid

- Using the Micromegas grids that were specially designed for TPX3

- Mount the primary grid on a bare TPX3 chip
  - Only SiN protection
  - Attaching with Araldite by glue wetted pillars
- Mount the gating grids on top of the primary grid
  - Attaching with Araldite by glue wetted pillars
- => ≈ 60 μm distance between the grids

- We might increase this to ~ 1 mm by using a G10 frame
- *But any distances between 60 μm and 1 mm will be very hard or impossible to realize*





Available Micromegas frame
Holes 55 x 55 μm pitch

Testing the gating grid

- Using the non-attenuated UV laser beam
  - We probably have to illuminate the full surface of the drift cathode to get sufficient primary electrons
  - (in the 8-quad testbox we were using the ionization of 8 chips)
- We might have to replace the existing gas envelope of conducting Semitron 490 HR
  - Might have a too unstable cathode current
  - Alternative Ertalyte gives microdischarges
- Challenge to measure a much reduced ion backflow