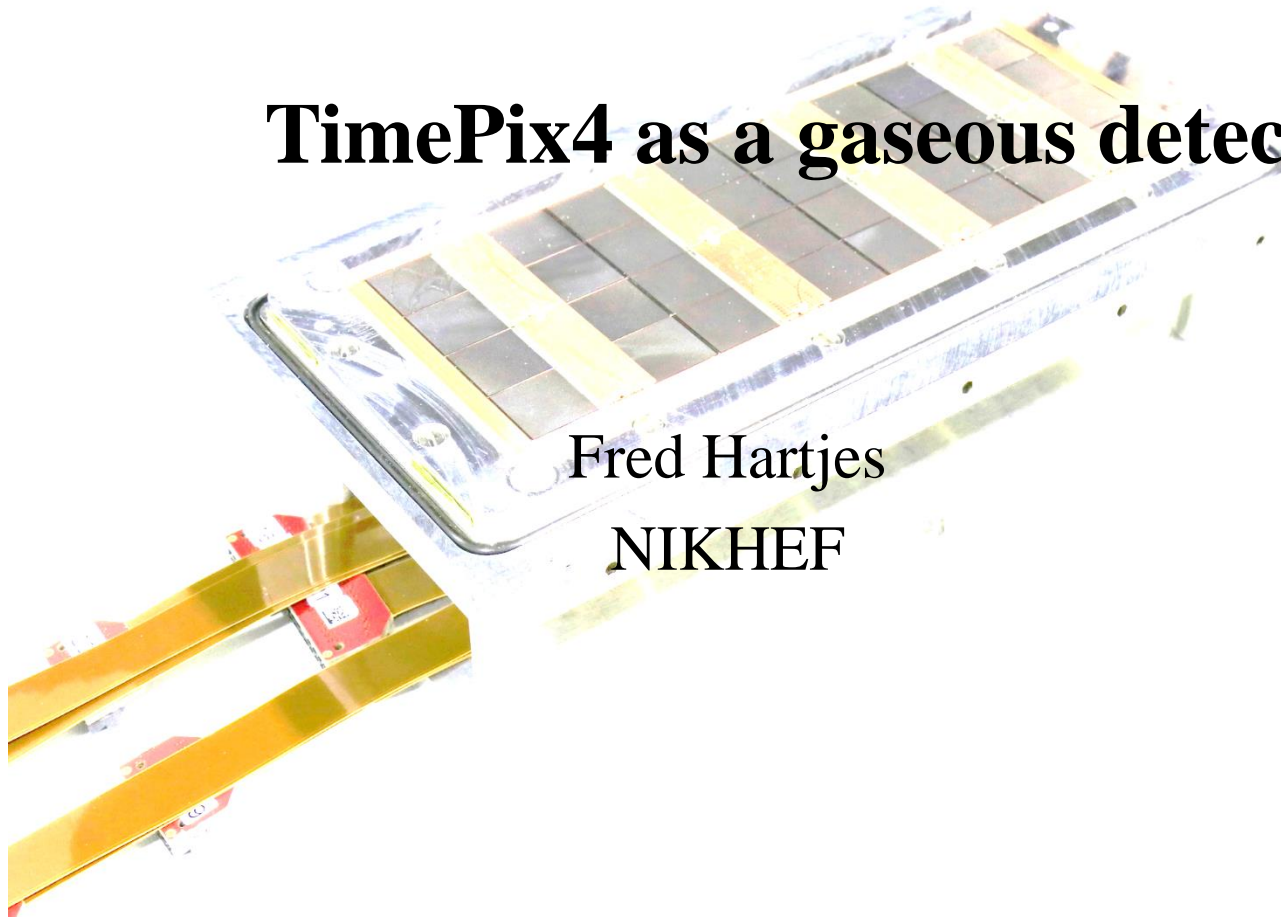


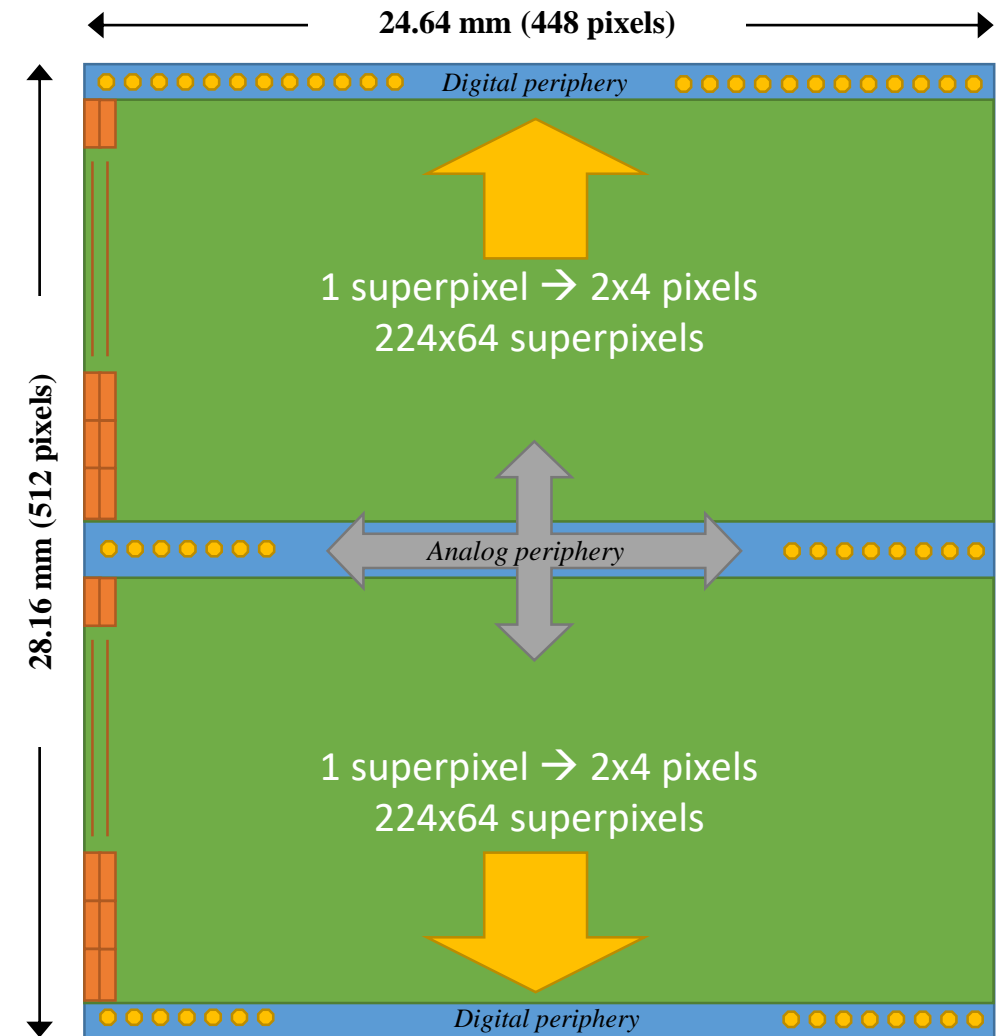
TimePix4 as a gaseous detector

Fred Hartjes
NIKHEF



Layout

- 512 x 448 pixels
- Cell size 55 x 55 μm (on external surface)
 - 55 x 51.875 (internal)
- External pads also cover analog and digital periphery
- Using Through Silicon Via (TSV) connections multiple chips can be joined without any dead space (in case of silicon detectors)
- Die dimensions 28.215 x 24.695 mm (TSV)
- Using wire bonds 2 x 0.9 mm added on both sides
- Not all IO pads on both sides need to be connected
 - Only output lines are crucial

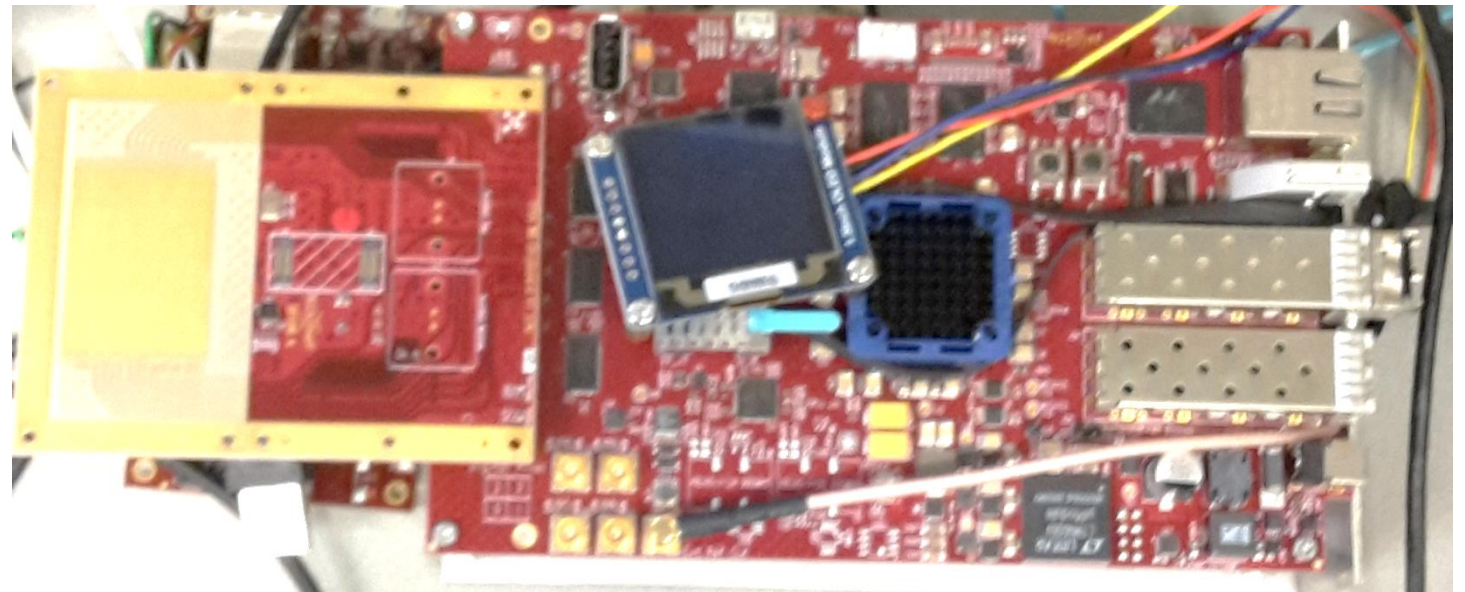
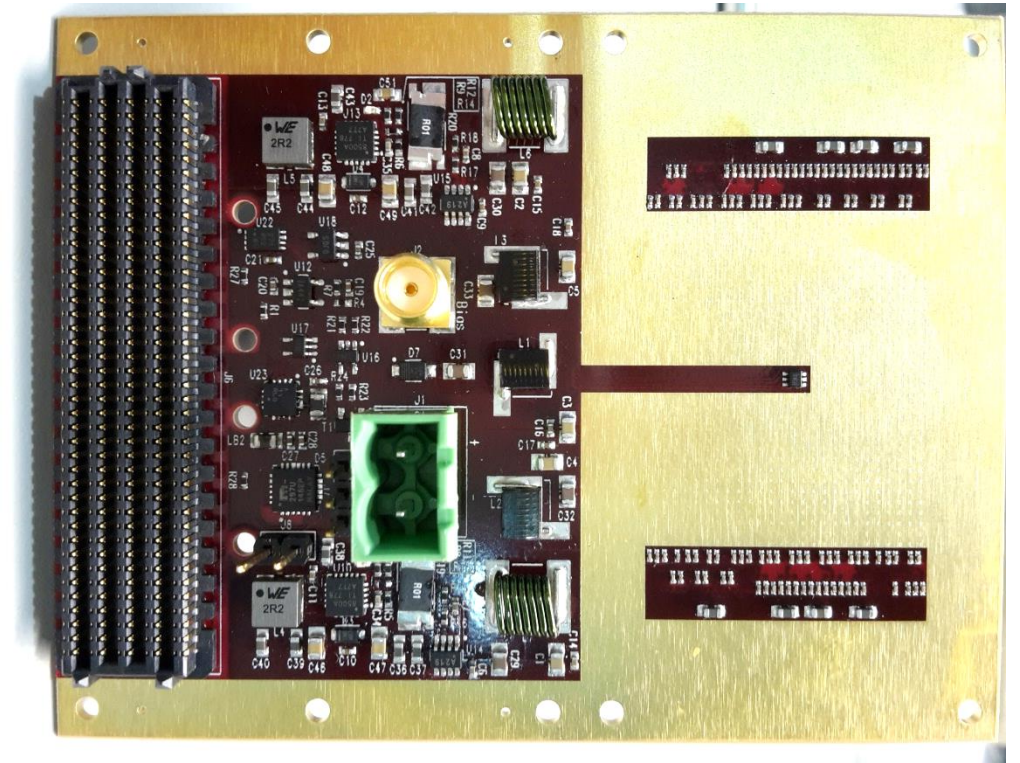


TimePix3 vs TimePix4

	TimePix3	TimePix4
# of wire bond pads	110 (92 used)	147 (~ 100 will be used)
Pixel pitch (μm)	55 x 55	55 x 55
Wire bond pitch (μm)	73 (signals) /146 (power)	165
Minimum threshold	500 e^-	500 e^-
LV power (digital + analog)	1.5 V	1.2 V
Active surface (mm^2)	198	694 (3.5 x TPX3)
RO rate per unit of active surface	< 43 Mhits/ cm^2/s	357.6 Mhits/ cm^2/s

Status

- Submit week November 11, 2019
- First chips available: ~ end January 2020
- Hope to get one/ two edge chips
 - Electrically not usable
 - Good for designing detector
- Chipboards exist (Nikhef design by Bas)
 - Twin power supply (digital and analog completely separated)
 - Chipboard plugged on new SPIDR
- Maybe easy to add a protection layer on a loose chip
 - Yevgen in Twente?



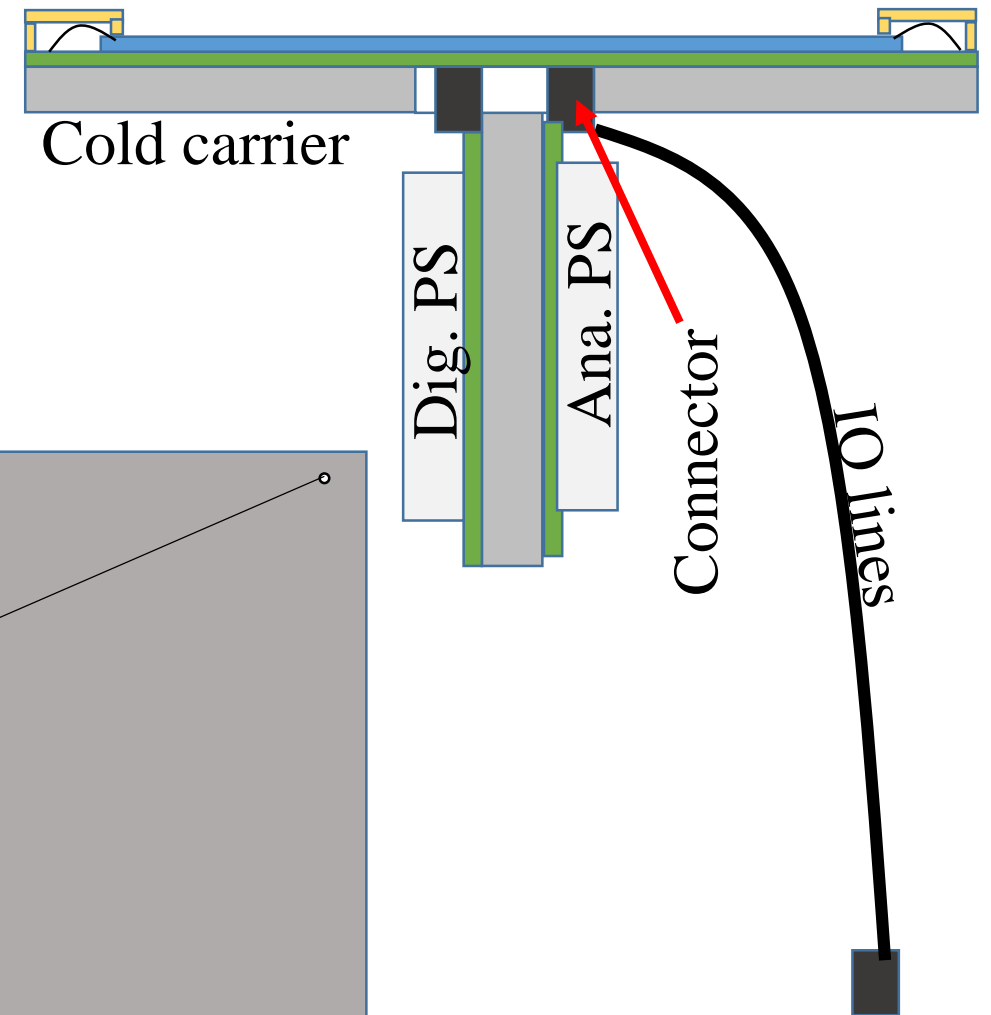
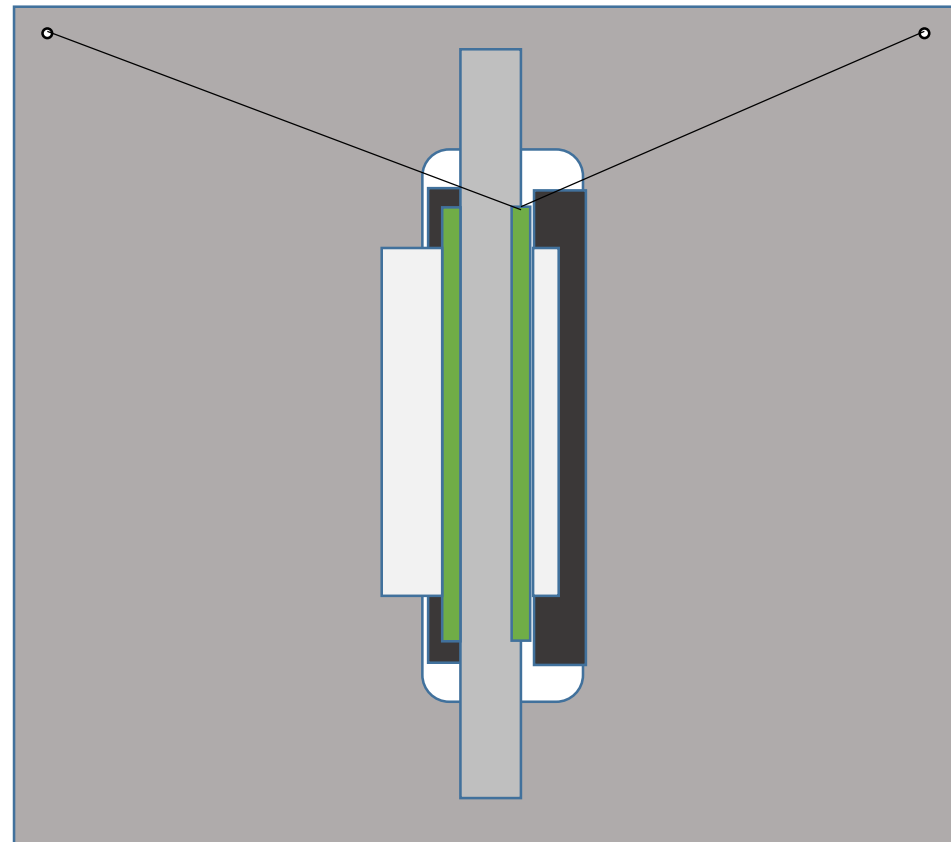
Adding InGrid

- Total active surface: 694 mm²
- Add surrounding dyke of 165 μm wide
- Add central dyke of 220 μm wide
- Divide the grid into two halves
 - => reduction of grid capacity
 - => less risk on discharge damage
- Add two 1 mm² pads for grid voltage connection
- => 24.7 mm² lost from active surface (3.5%)
- Final active surface using InGrid: 669 mm²



Construction detector from TPX4

- Aim for single chip detector
- QUAD => SINGLE
- Using more chips has no advantage
 - Always one LV PS per chip needed
- More chips implements:
 - More complex PCB
 - For ILD: more chips => more dead space on a module
 - Wire bonding more difficult
 - Assembly more critical
 - => lower yield
- Avoid using flexes
 - Nuisance during assembly
 - May make PCB more expensive



Total single dimensions and active surface

- On each side (top and bottom)
 - 0.9 mm wirebond extension
 - 3.5 mm for PCB (estimated) ??
- **Length** $29.96 + 2 \times 3 \approx \mathbf{37.0 \text{ mm}}$
- **Width** **24.695 mm**
- (Present quad: 39.6 x 28.38 mm)

- \Rightarrow total detector surface 914 mm²
- Active area 669 mm²
- $\Rightarrow 669/733 = 73.2\%$

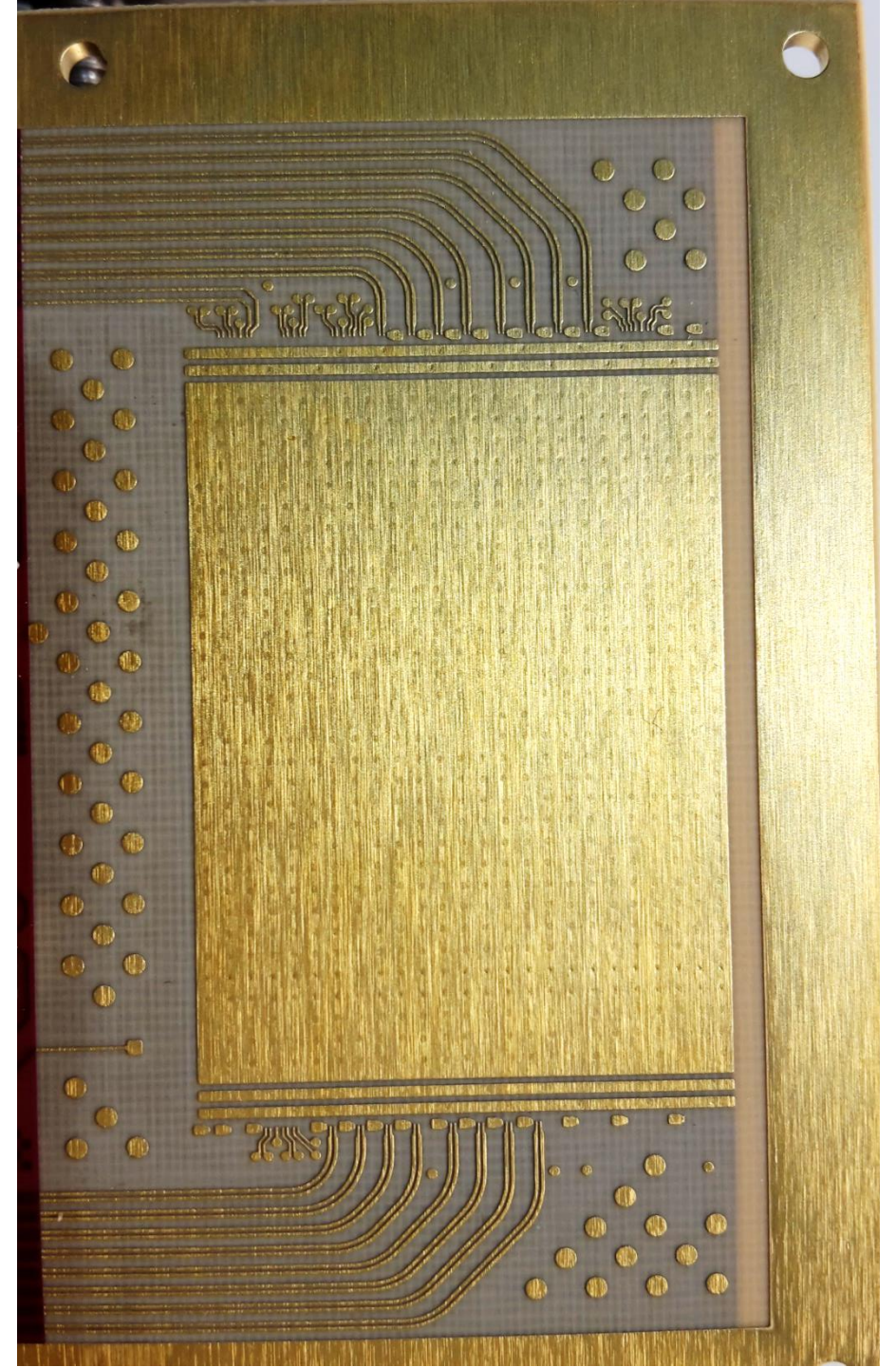


Advantages single (TPX4) over quad (TPX3)

- A bit improvement of the sensitive area (73 vs 69%)
- ~45% less chip-to-chip boundaries for a large detection surface
- Less bonding pads (368 vs ~ 100)
- Larger distance bonding pads (165 vs 73 and 146 μm)
 - \Rightarrow wirebond PCB may be much cheaper
- DAQ may be cheaper and simpler
 - No concentrator needed
 - 8 x faster readout rate
- With single we will profit for the experience from quad
 - Simpler wirebond board (flex and LV PCB separate)
 - No remachining of produced wirebond board
 - Improved assembly method of HV grid wires

How to proceed?

- We may start with putting a loose Micromegas foils on a bare chip
 - Foils of 12.6 x 13.1 mm (229 x 239 pixels) available
 - Interesting for the chip debuggers: real physical signals (not easy to get in another way on a short term)
- Adding a protection layer may be done in a quite short time
 - Yevgen in Twente?
 - We may have this already summer 2020
- Next steps much more time consuming
 - Summer 2021? wafers available for InGrid depositing
 - Summer 2022 or later: first successful chips with Ingrid
 - 2023 first prototype detector with TimePix4
 - Time estimates may be too optimistic
 - Could easily be 1 – 2 years later



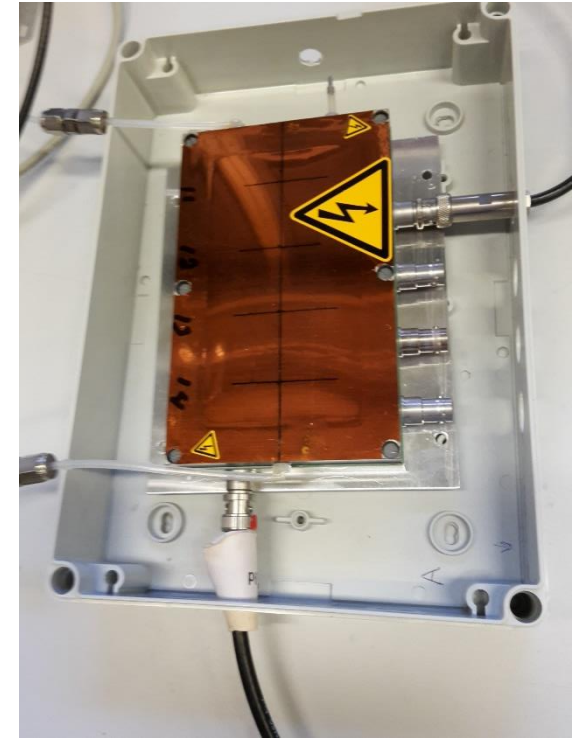
What about TSV (Through Silicon Via)?

- TimePix3
 - Incorporated in the design, but never realized

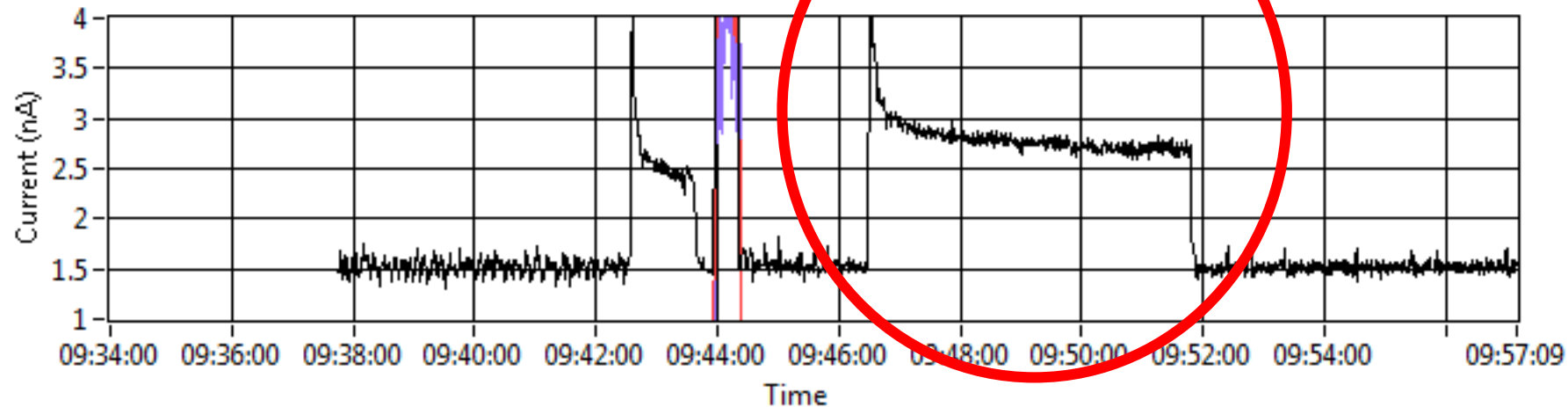
- TimePix4
 - Incorporated in the design.
 - Not an issue for silicon trackers
 - Dead area avoided by overlap
 - Relevant for optical and gaseous detectors

Ionic drift

- Ar + 1.2% CS₂
- There is gas gain, grid voltages comparable with T2K
- Good gain at -370 V grid
- Normal current under 90Sr source
 - Large charging up effect (factor 4)
 - Same with T2K



Current graph



CH1	
CH2	
CH3	
CH4	

SPARE

	Quad (TPX3)	Single (TPX4)
Total surface (mm2)	1124	914
Active surface (mm2) / (%)	774 / 68.9	669 / 73.2