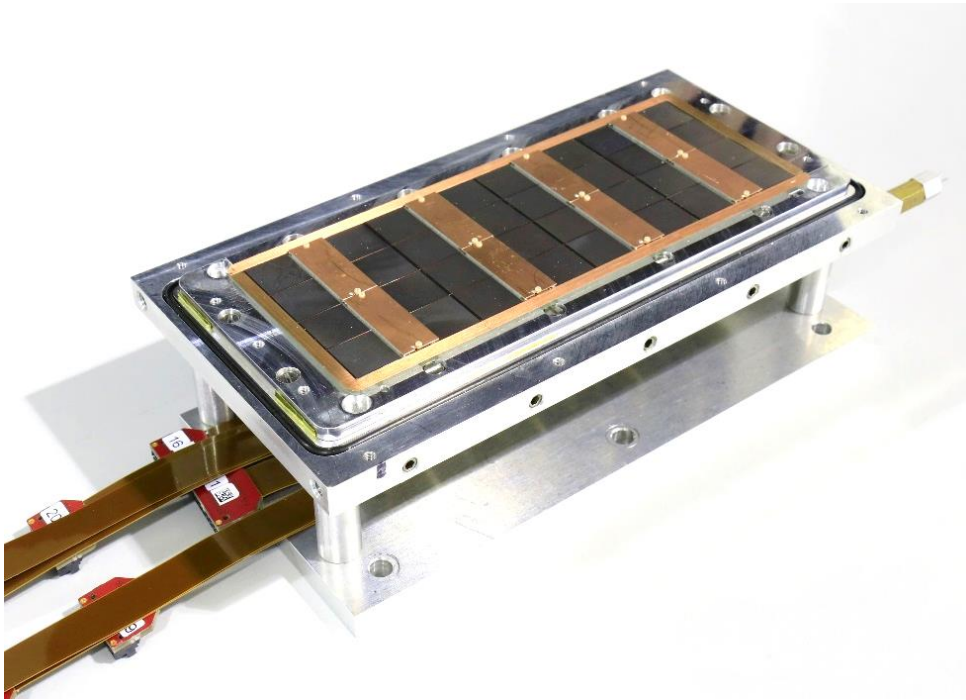




Construction of an eight-quad module



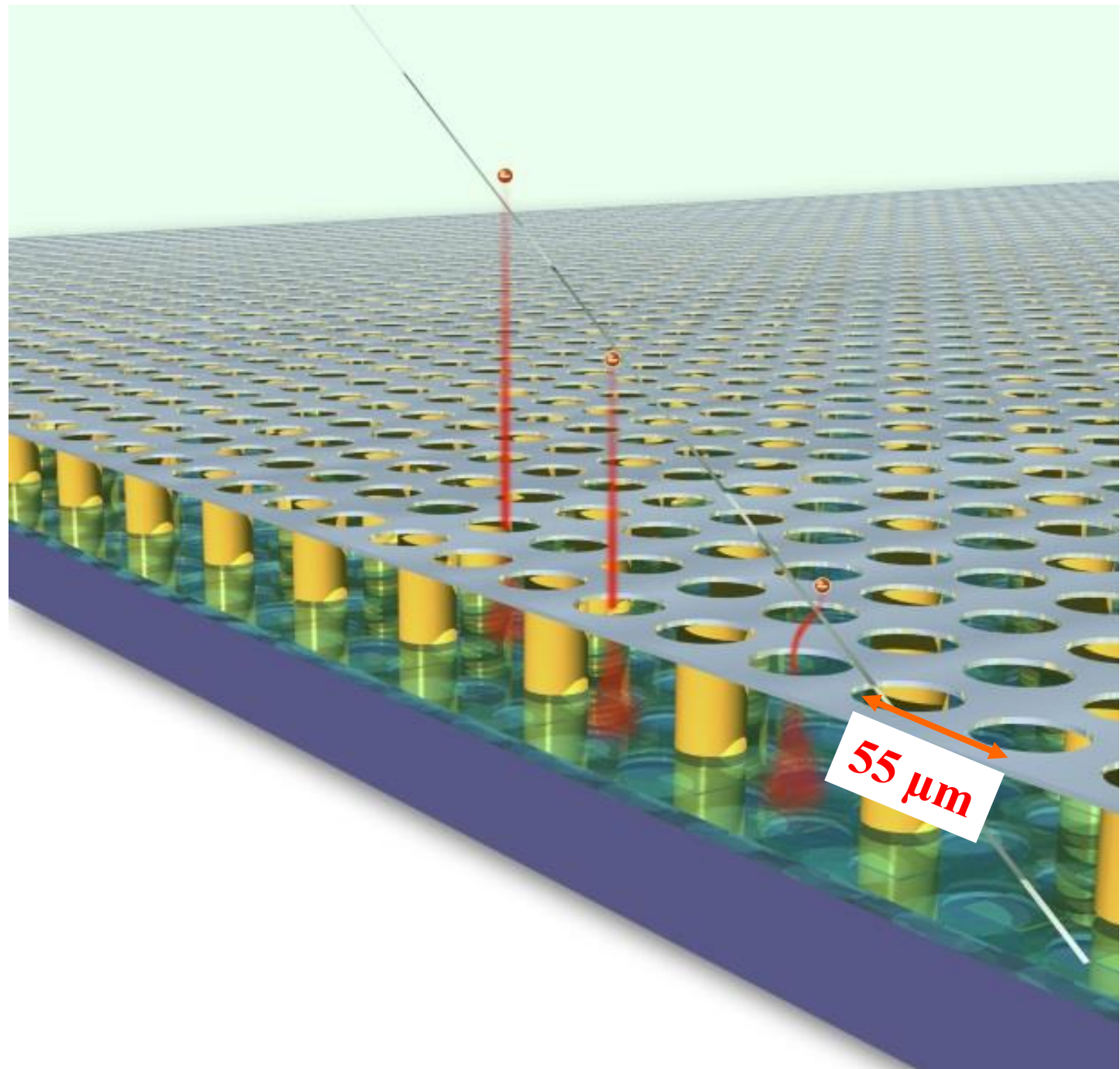
Fred Hartjes
NIKHEF

LC-TPC collaboration meeting
DESY, January 14, 2020

GridPix technology

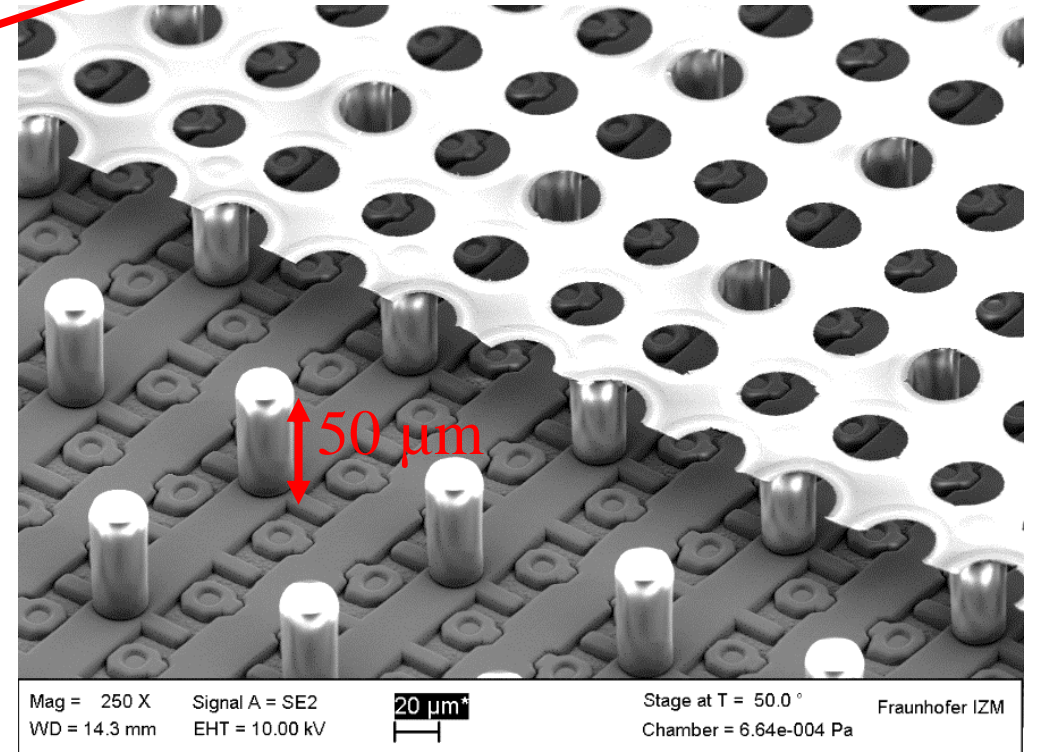
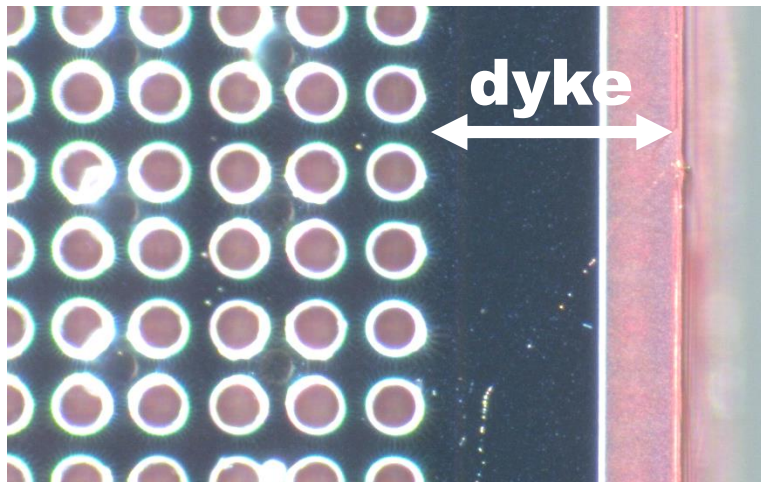
- Pixel chip with integrated Micromegas
- => **InGrid**
- Grid set at negative voltage (300 – 600 V) to provide gas amplification
- High granularity (55 x 55 μm)
- => mostly detecting **single electrons**

GridPix chip



TimePix3 equipped with InGrid

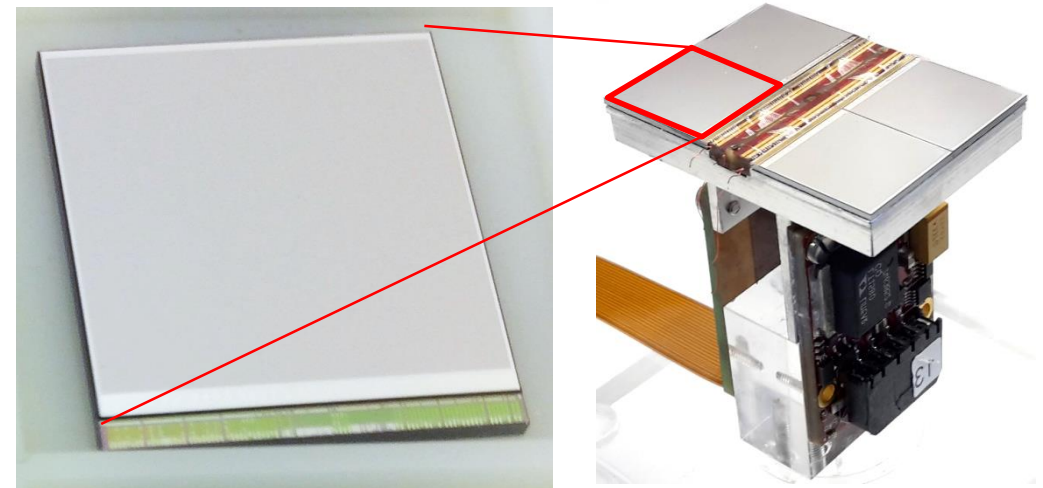
- Wafer post-processing at IZM Berlin
- Aluminium grid (1 μm thick)
- 35 μm wide holes, 55 μm pitch
- Supported by SU8 pillars 50 μm high
- Grid surrounded by SU8 dyke (150 μm wide solid strip) for mechanical and HV stability



Fred Hartjes

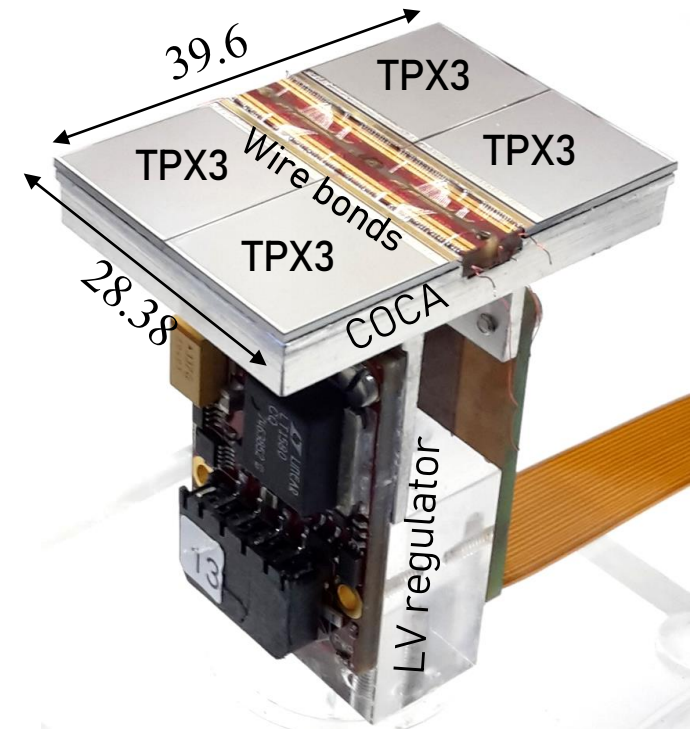
Quad: four TimePix3 unit

- Services under the detector surface of 28.38 x 39.6 mm
- => may be extended unlimited in the XY plane
- 12 working QUADs have been produced



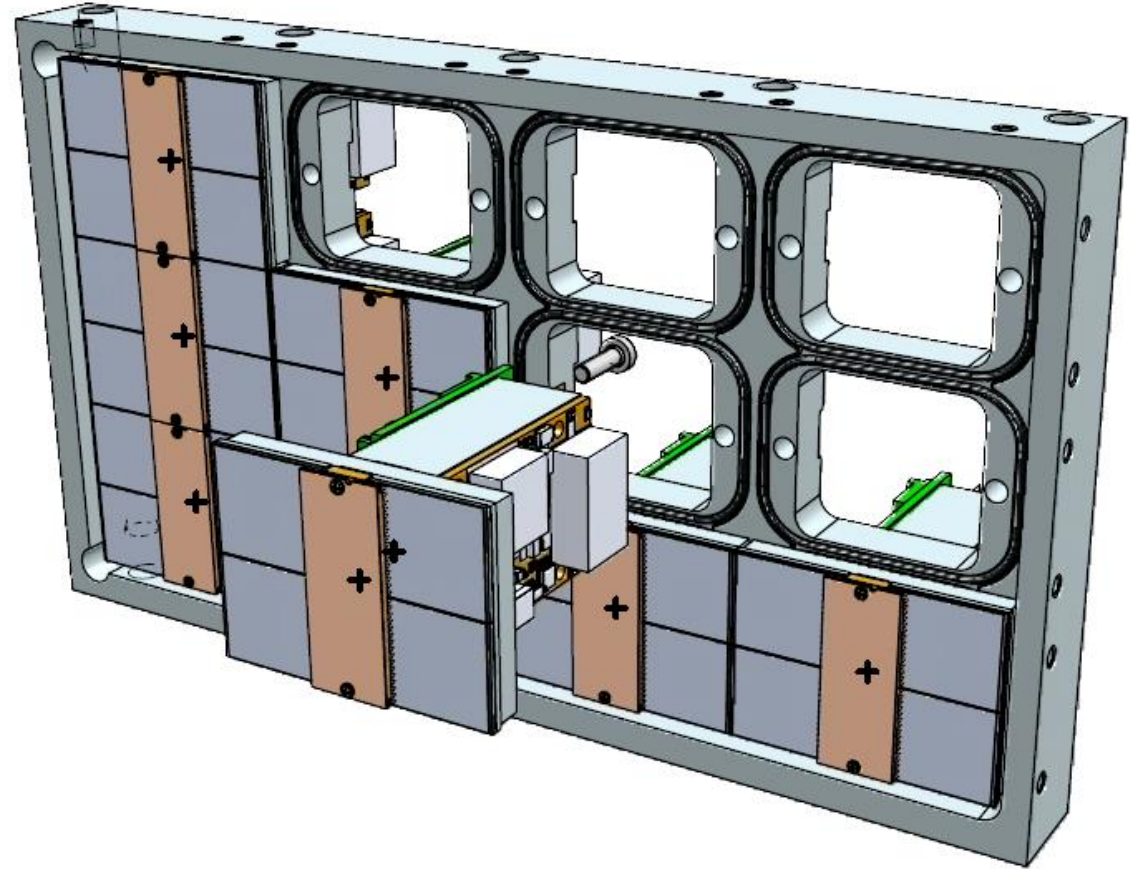
Construction of the quad

- A four TPX3 chip unit, top surface 11.24 cm²
- Chips mounted on a base plate (COLD CArrier) under high precision
 - < 20 μm mounting of the chips
- Wirebonding to a 6 mm wide PCB in the centre
- Area for connections IO was minimized
 - Maximises active area (68.9%)
- Two electronic boards under the baseplate
 - LV supply
 - HV board (grid and guard)
- Kapton flex for IO signals
- To maintain a homogenous electric field, the wire bonds are covered by a central guard (omitted on the picture)



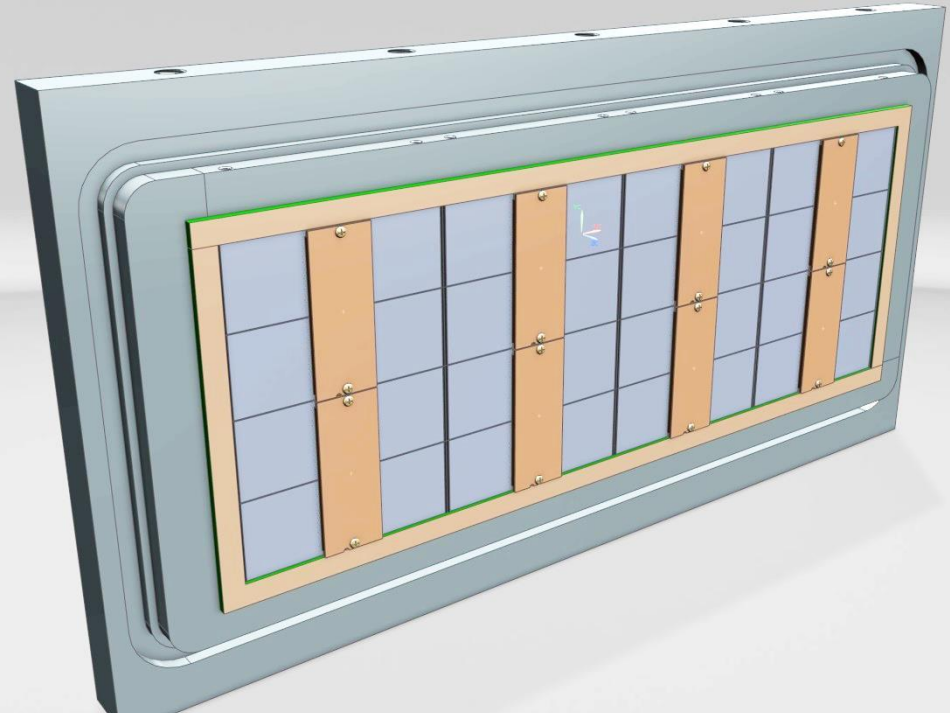
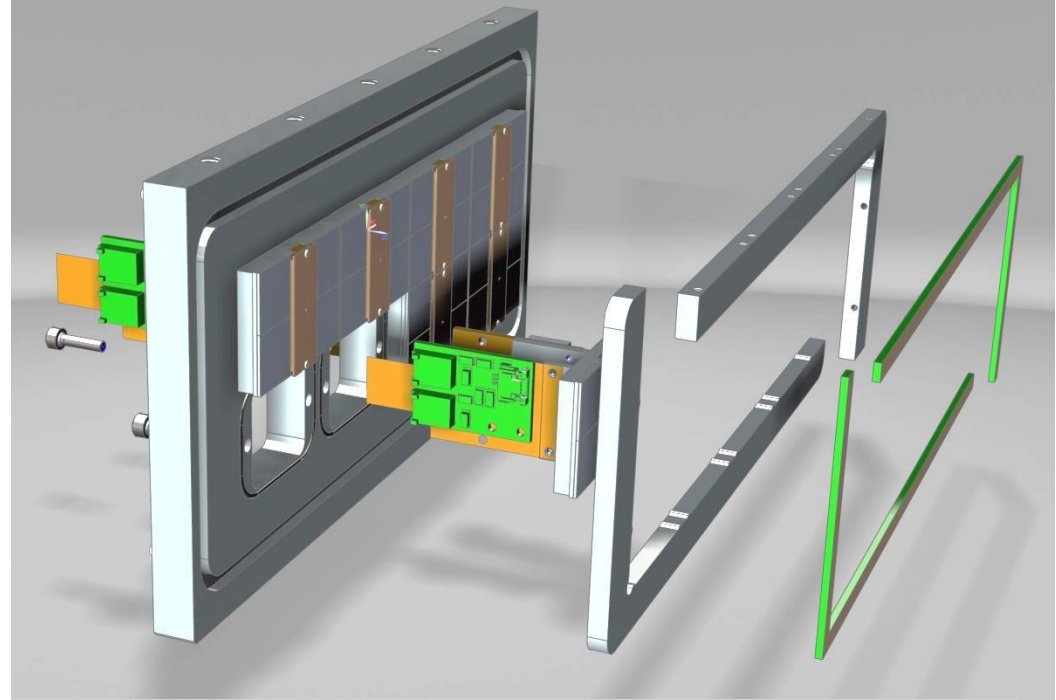
Extending the detection surface

- Basically the detection surface of a quad TPC can be extended unlimitedly
- Quads are mounted in holes on a solid cooling plate
- For practical reasons (handling) it is wise to limit the number of quads to a few tens
- The detection surface is made gastight, so we make the gas barrier under the COCA
 - => the electronics are outside the gas volume

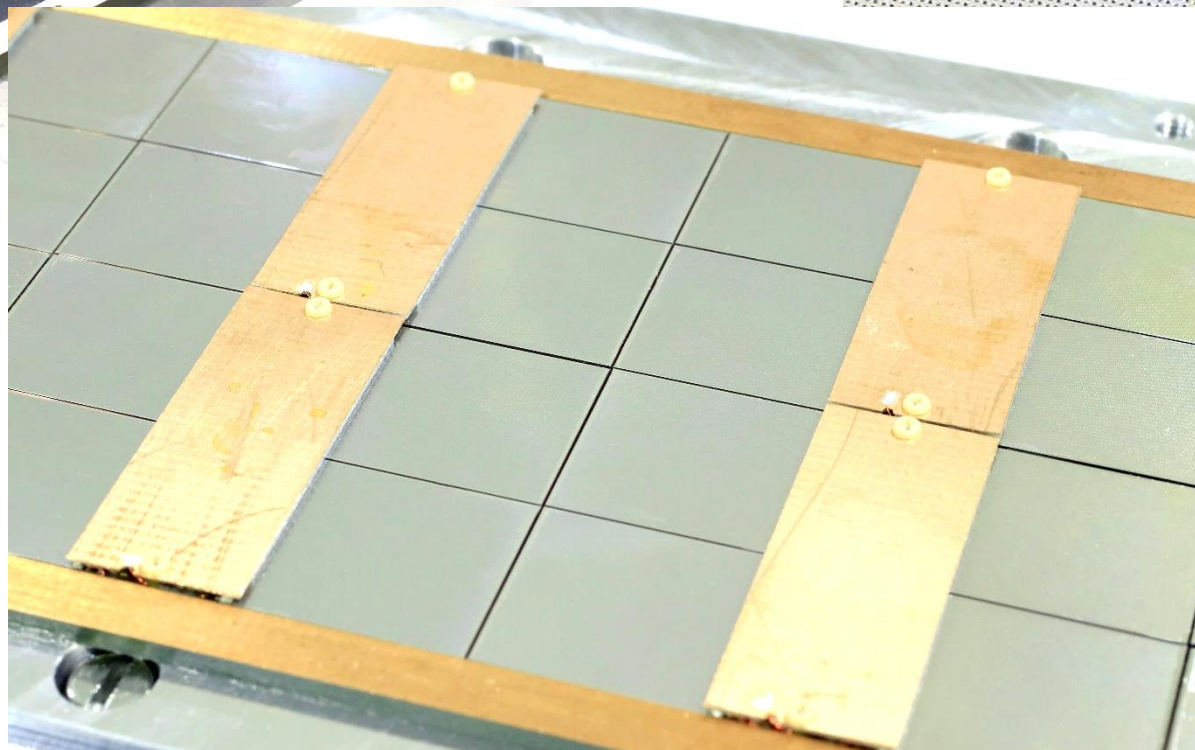
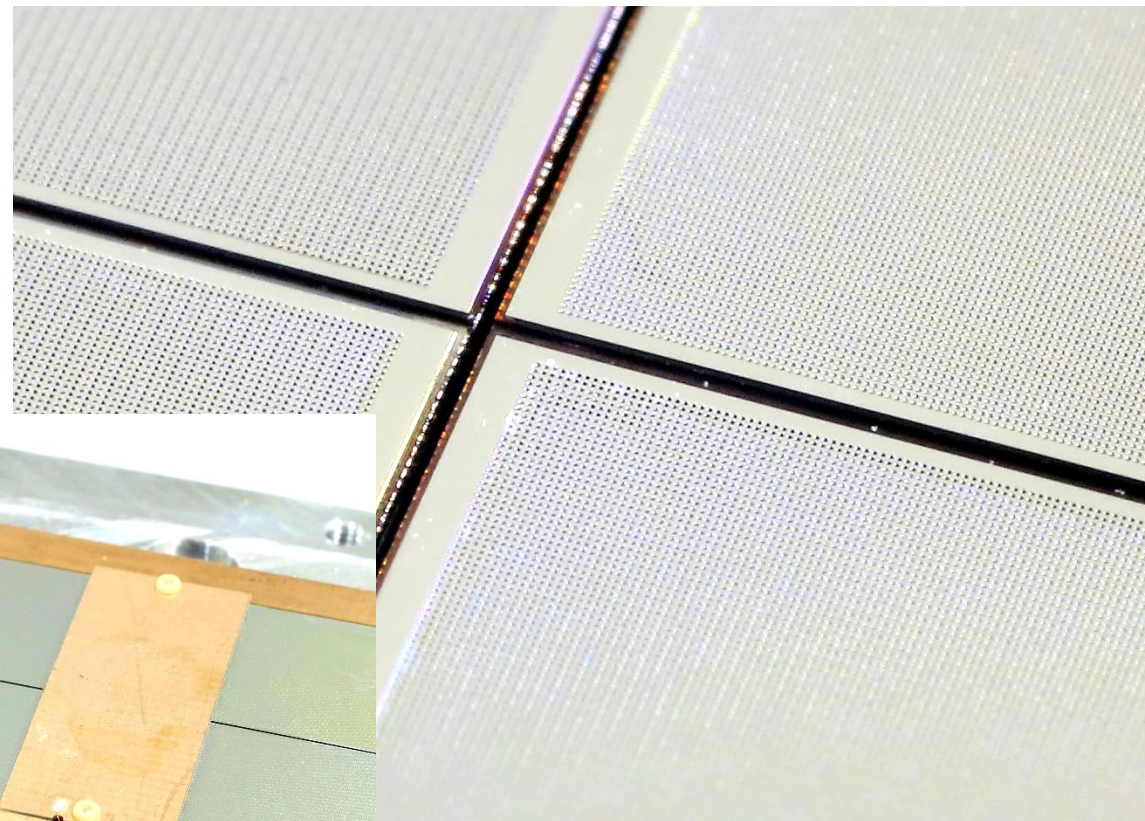
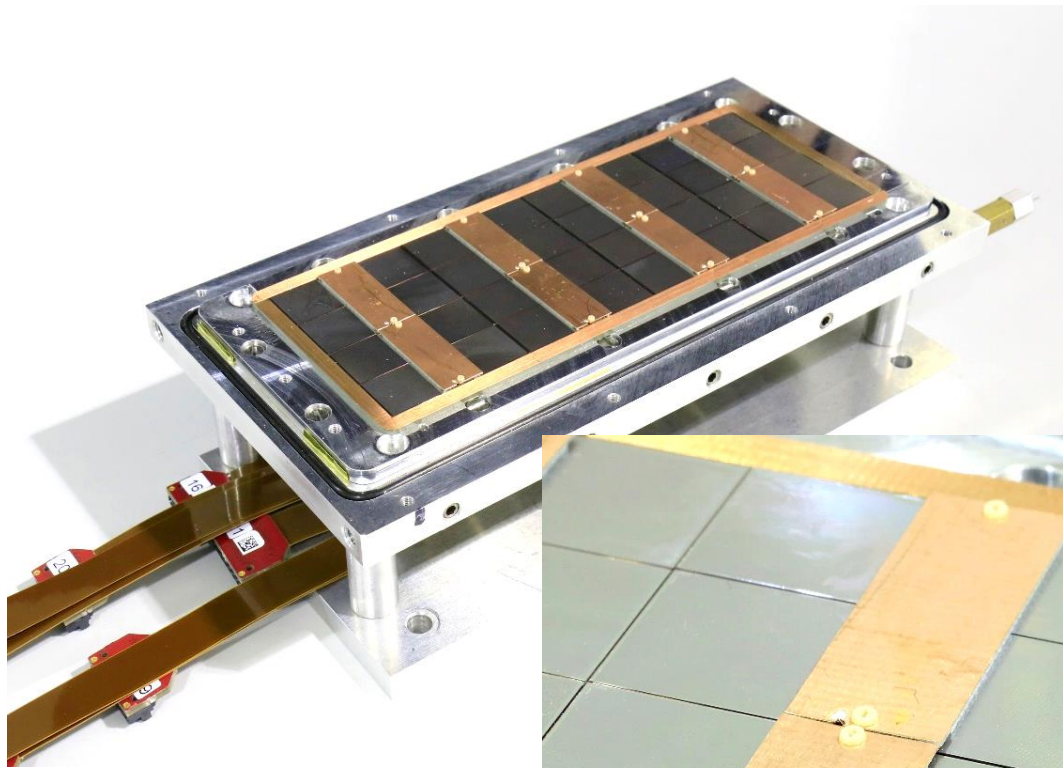


Design of the eight quad module

- Solid aluminium support plate with cooling channels
- Alignment by two L-shaped bars
 - One having reference notches to align the QUADs
 - One having compression screws to push the QUADs to the alignment bar
- 4 mm wide guard strips glued onto the L-bars
- Covering 90 cm² of which 62 cm² is active

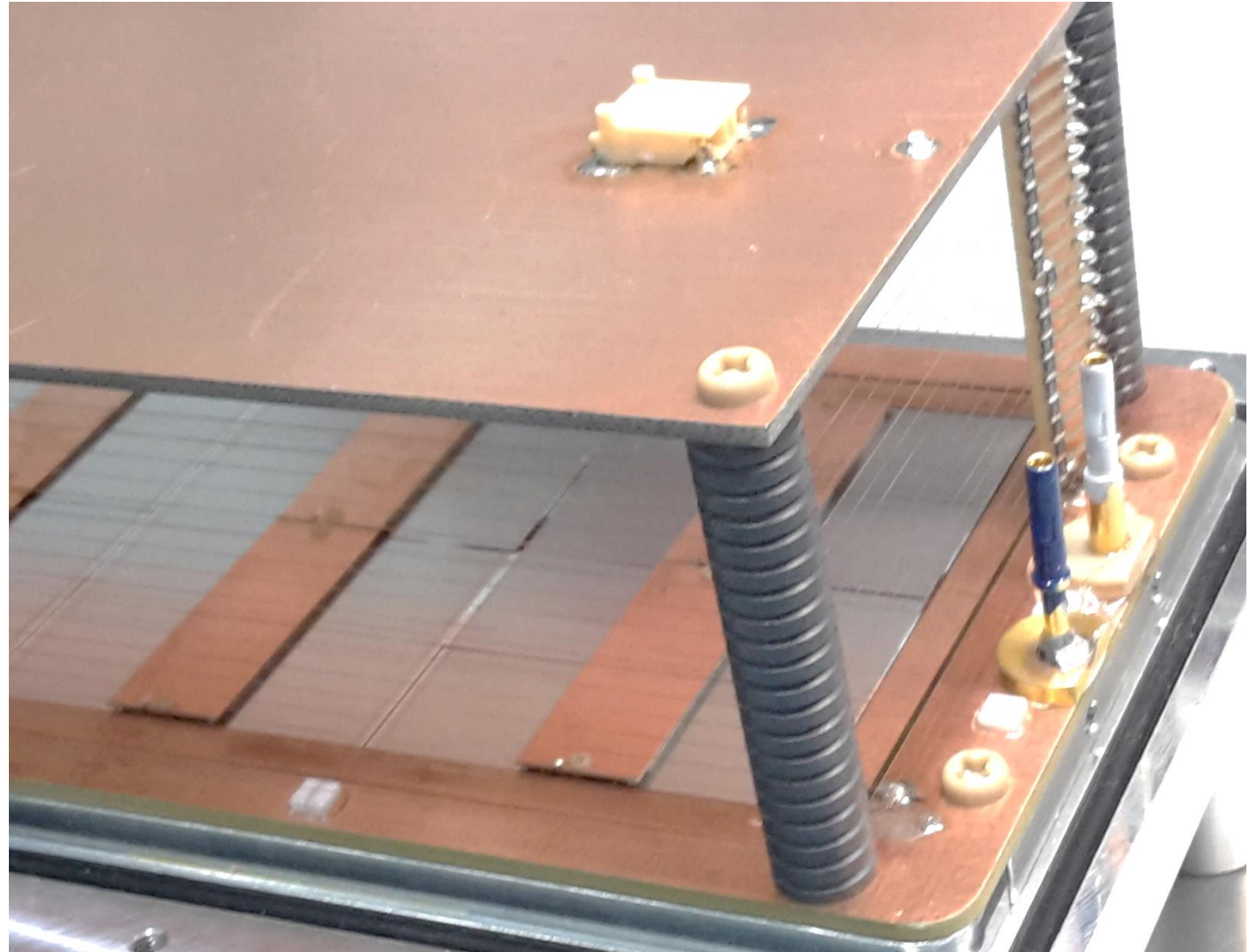


Eight-quad module has been realized



Adding a field cage to create a drift field

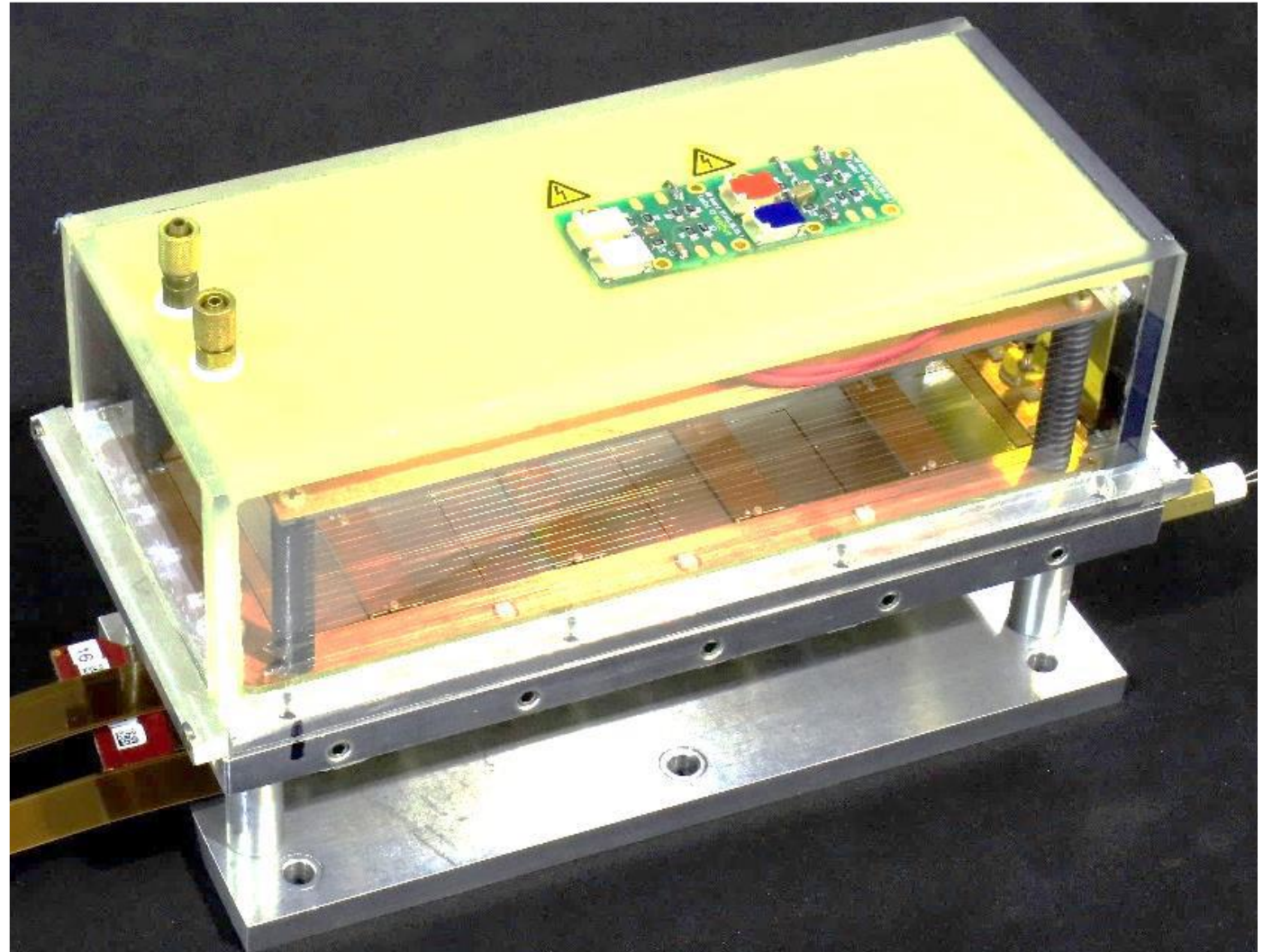
- 4 cm high drift space
- Terminated by wires to enable penetration of a laser beam



Fred Hargies

Completed testbox including the gas envelope

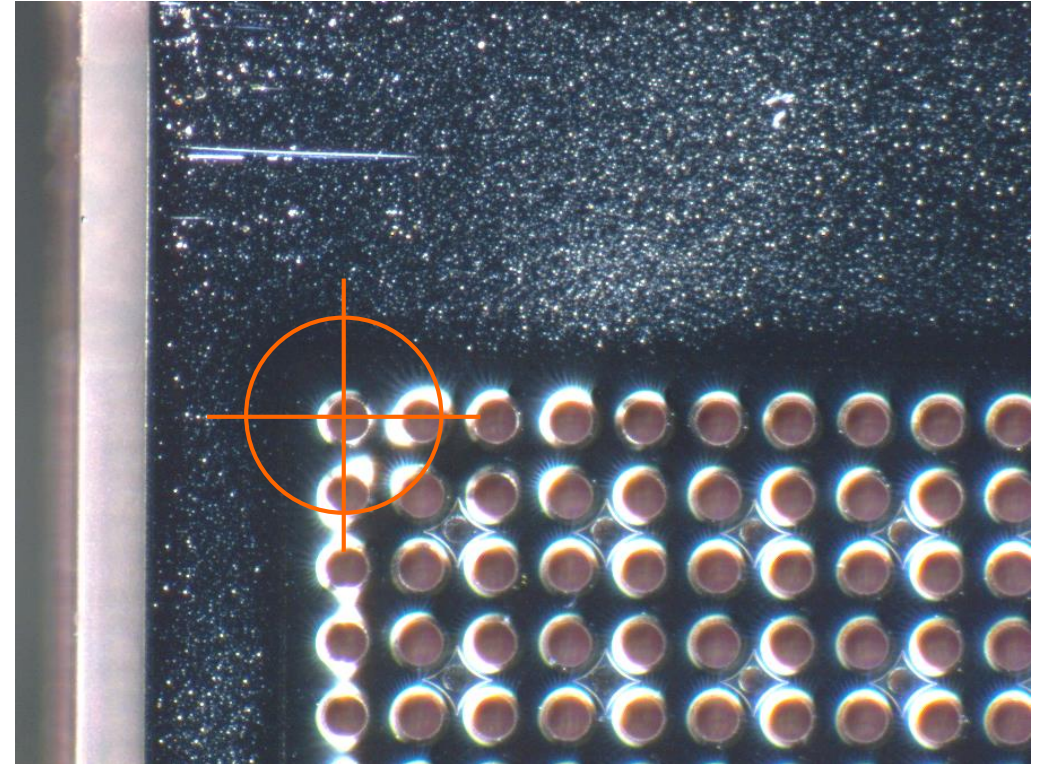
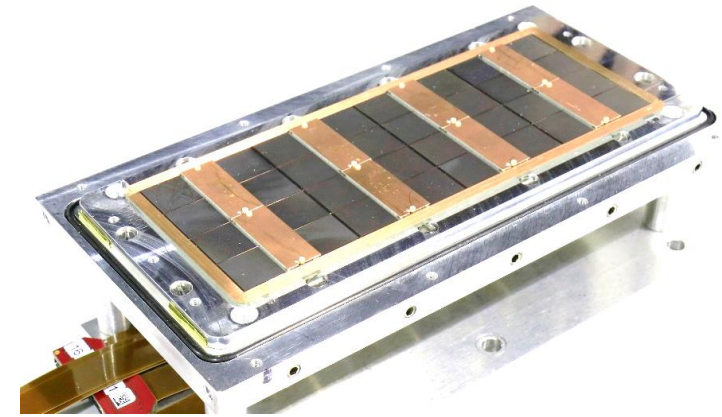
- Glass plates to enable laser measurements



Fred Hartjes

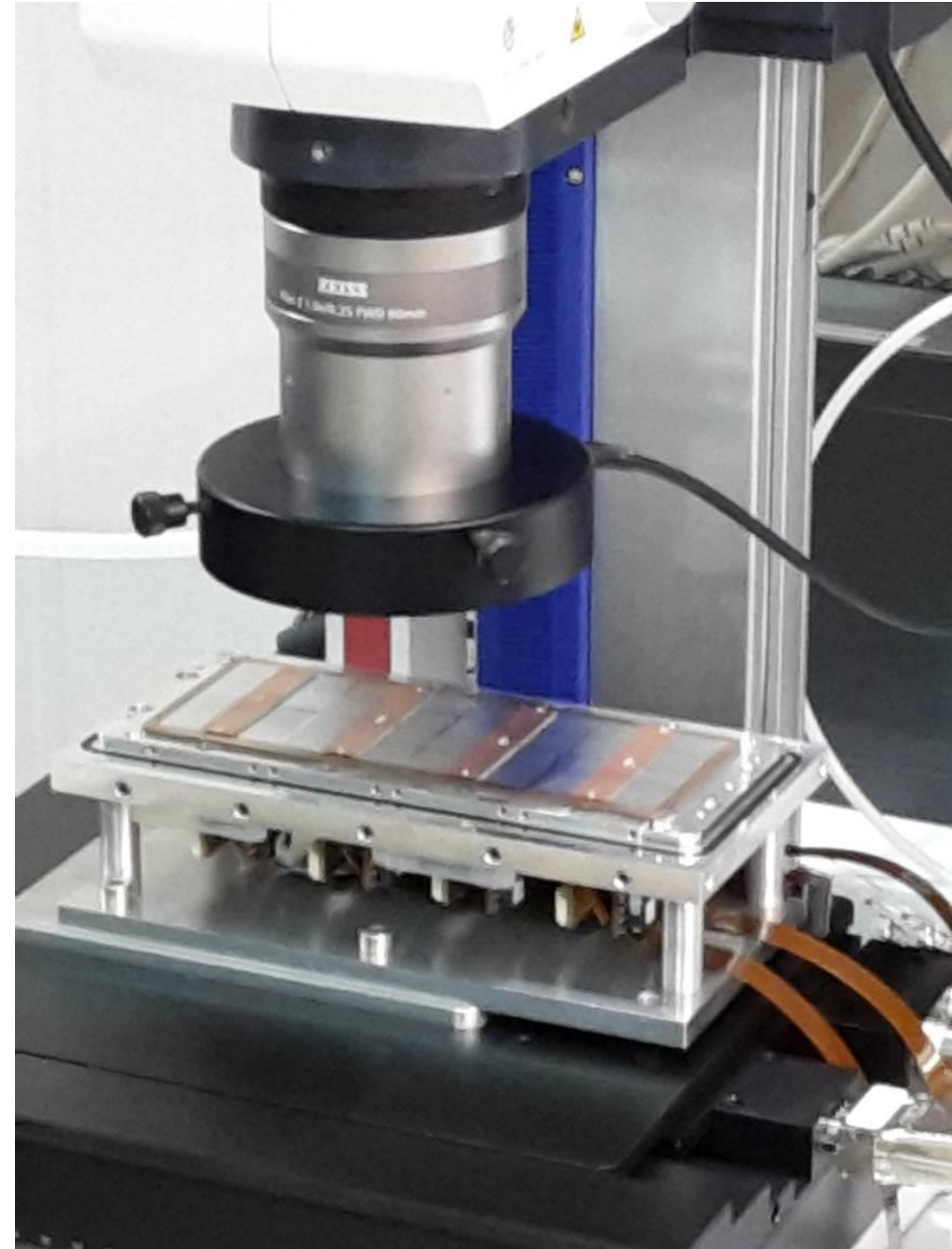
Creating a dataset of the position all chips

- The X/Y/Z/ ϕ coordinates of all 32 chips have been measured
- Each chip characterized by 3 points (grid holes)



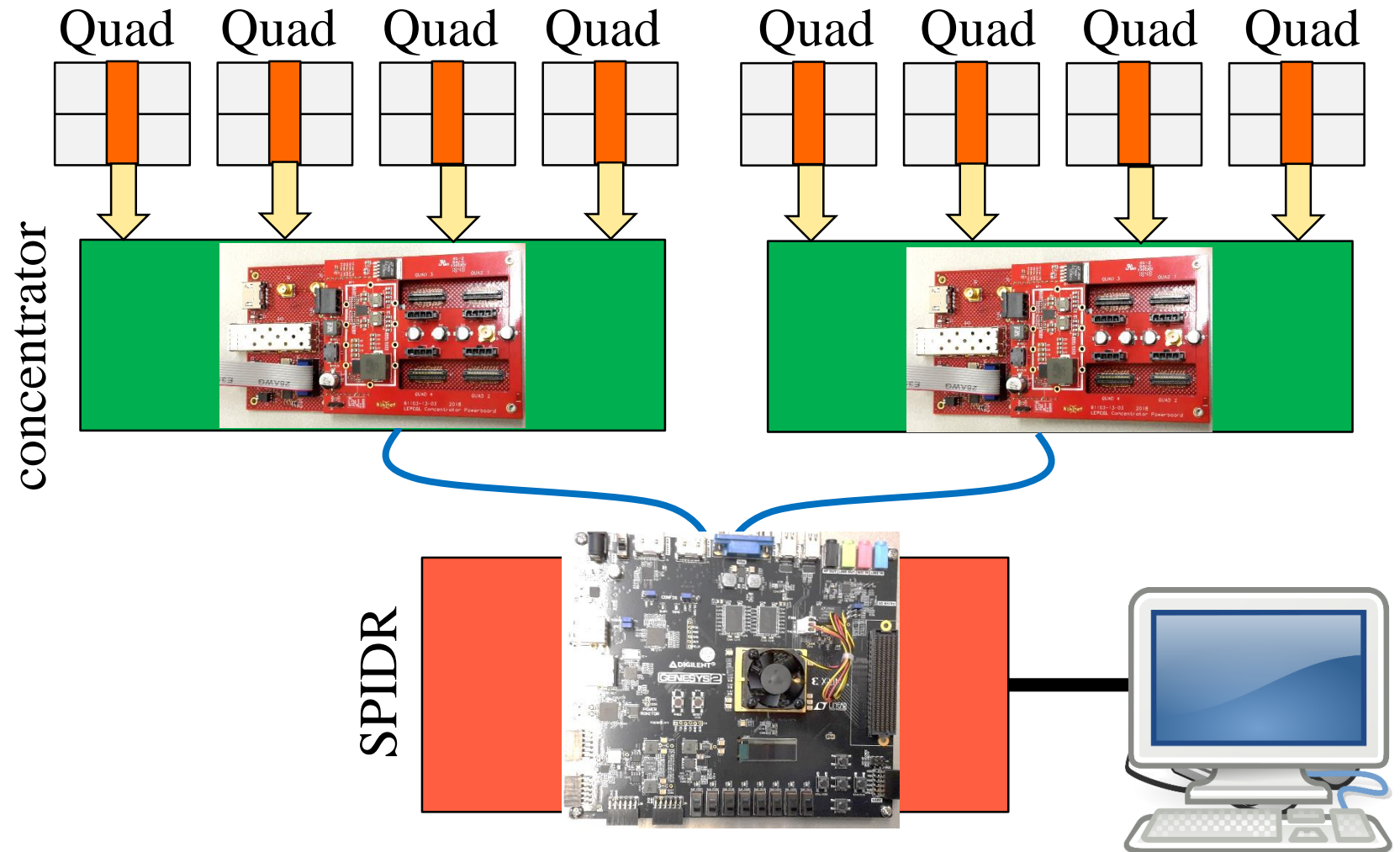
Measuring coordinates of all chips

- Use the alignment microscope with LabVIEW controlled XY stage
- Presently semi-automatic
- Method can completely automated using a remotely controlled microscope



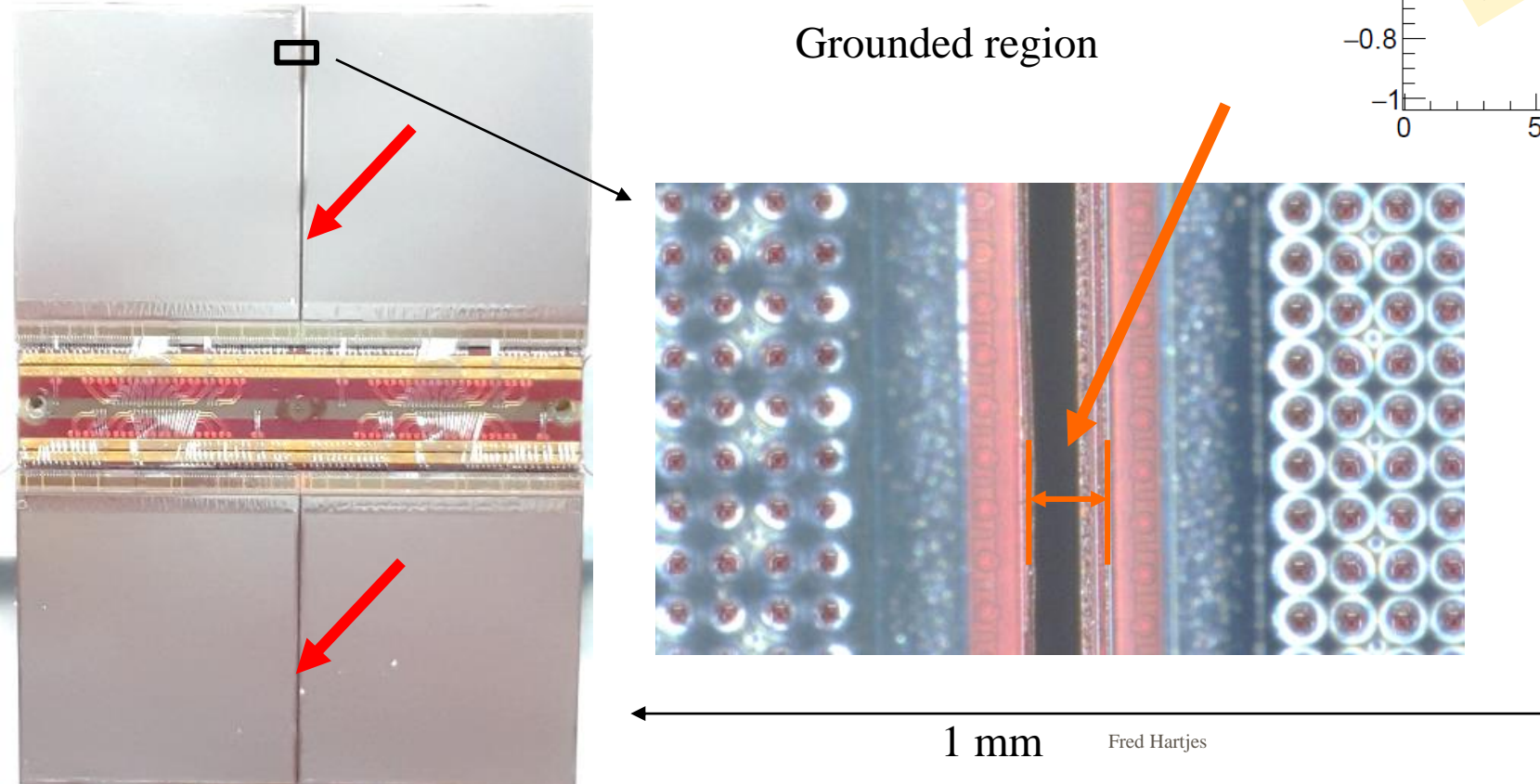
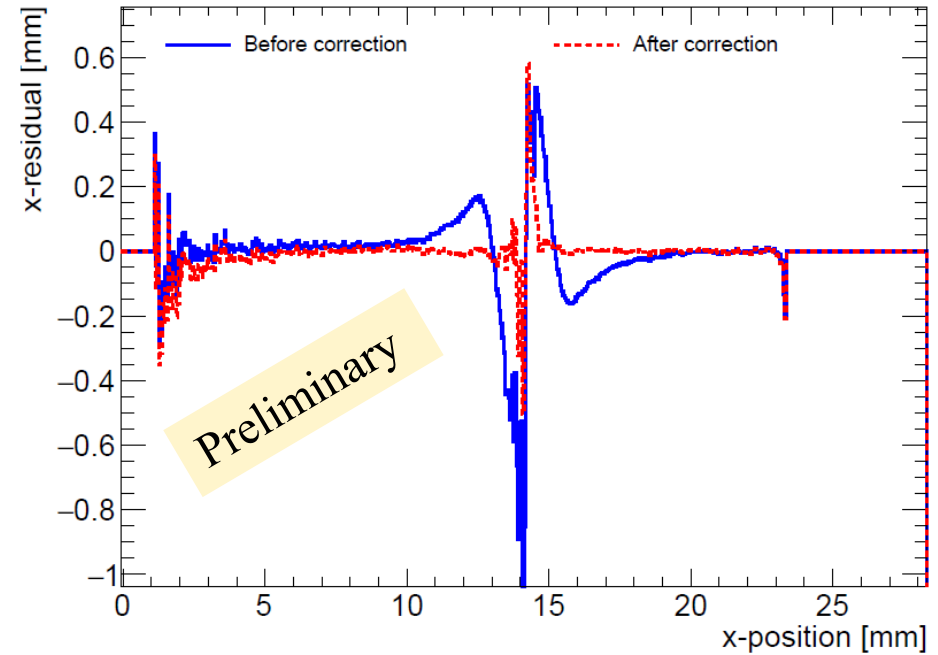
DAQ

- To read out 8 quads simultaneously, the IO flexes have to be connected to two concentrator boards
- Subsequently both concentrator boards are connected to a single SPIDR board by optical links
- Programming the firmware of the concentrator boards and SPIDR in progress
 - Near completion



QUAD edge deformations

- Discovered during Bonn testbeam in 2018
- Small deformations due to
 - Dead zone between chips
 - Grounded region between chips
- May be corrected by fitted correction function or adding proper guard electrode

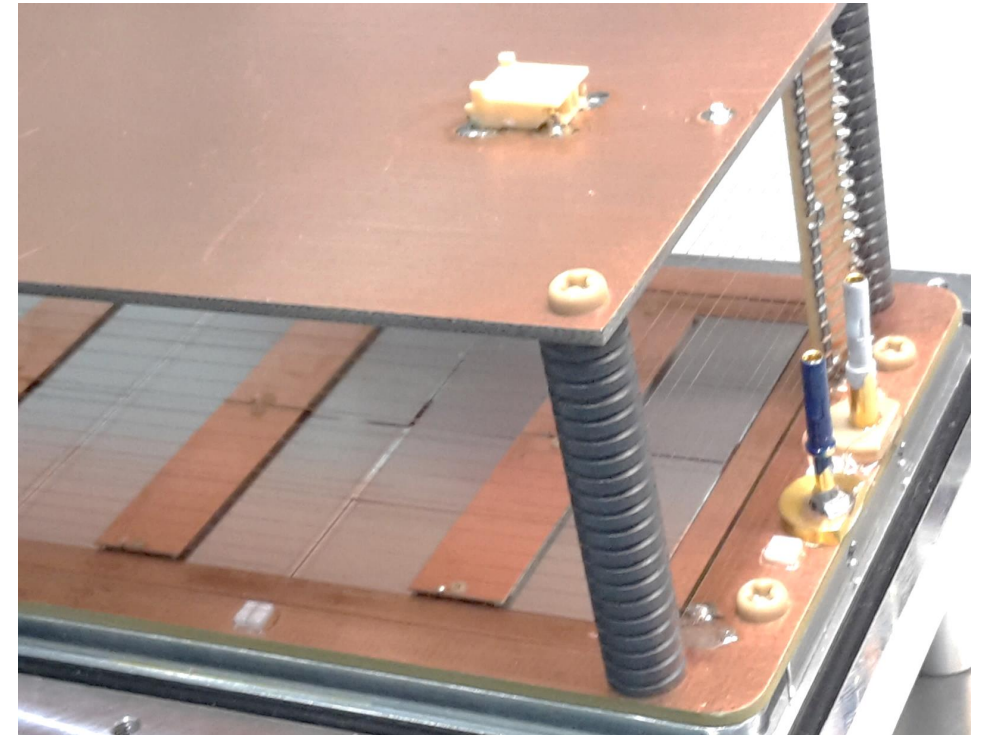
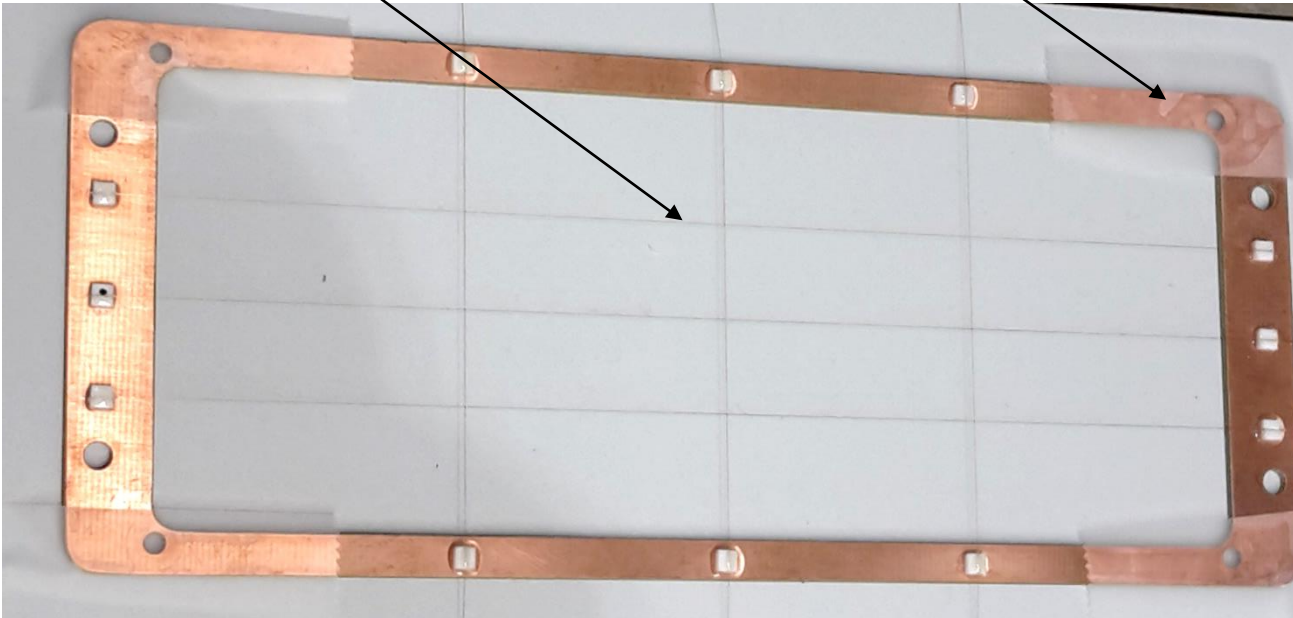


Improvement by additional guard wires

- Wires being glued on field cage frame
 - 1.1 mm above grids

Field shaping wire

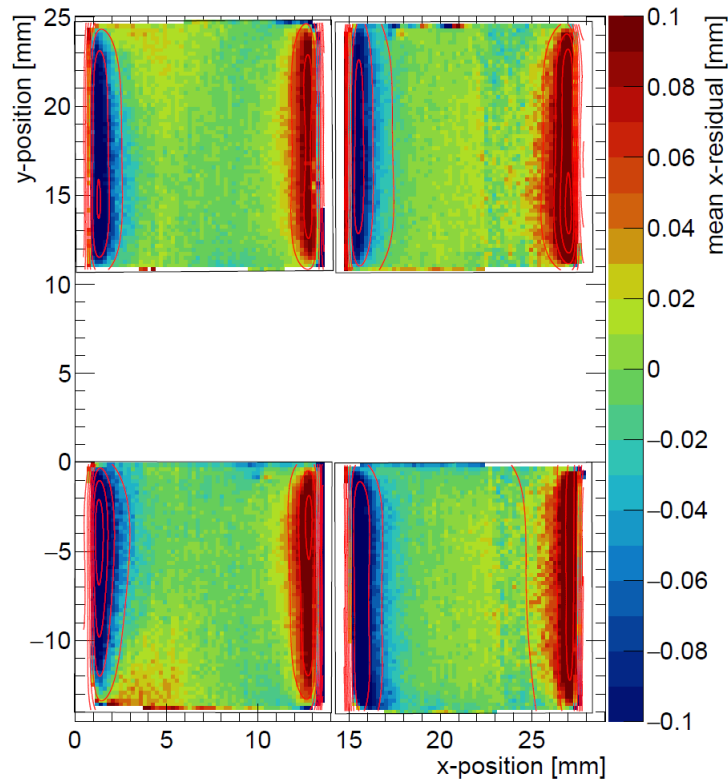
Field cage frame



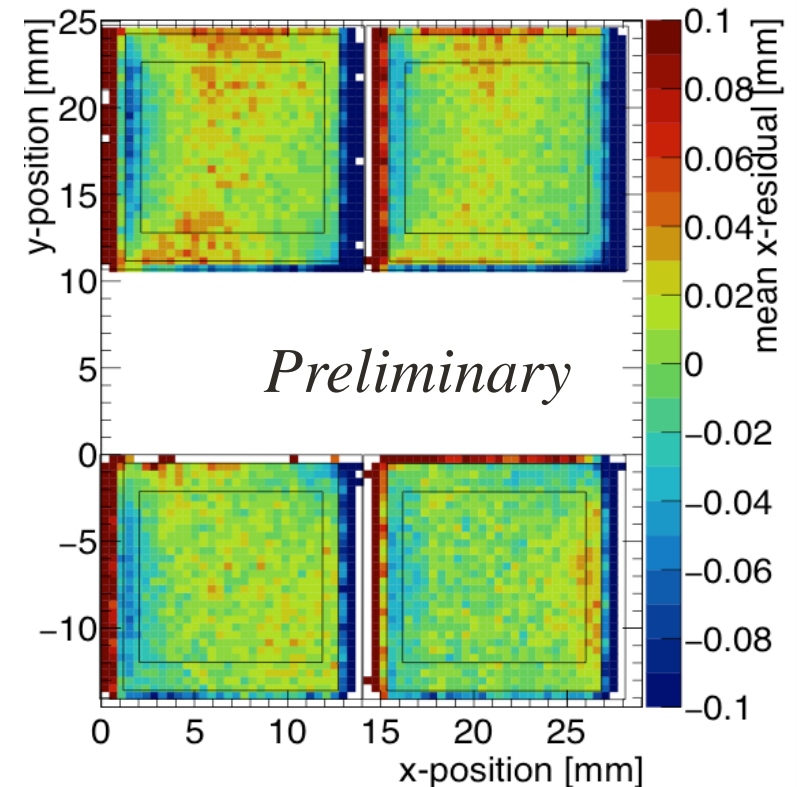
Effect of field shaping wires

- Wires ~ 1 mm above the grid
- Optimum voltage deduced from several scan with UV laser beam
- Potential 55 V more negative than grid voltage
 - 15 V more negative than deduced from drift field effect

Uncorrected (from test beam)

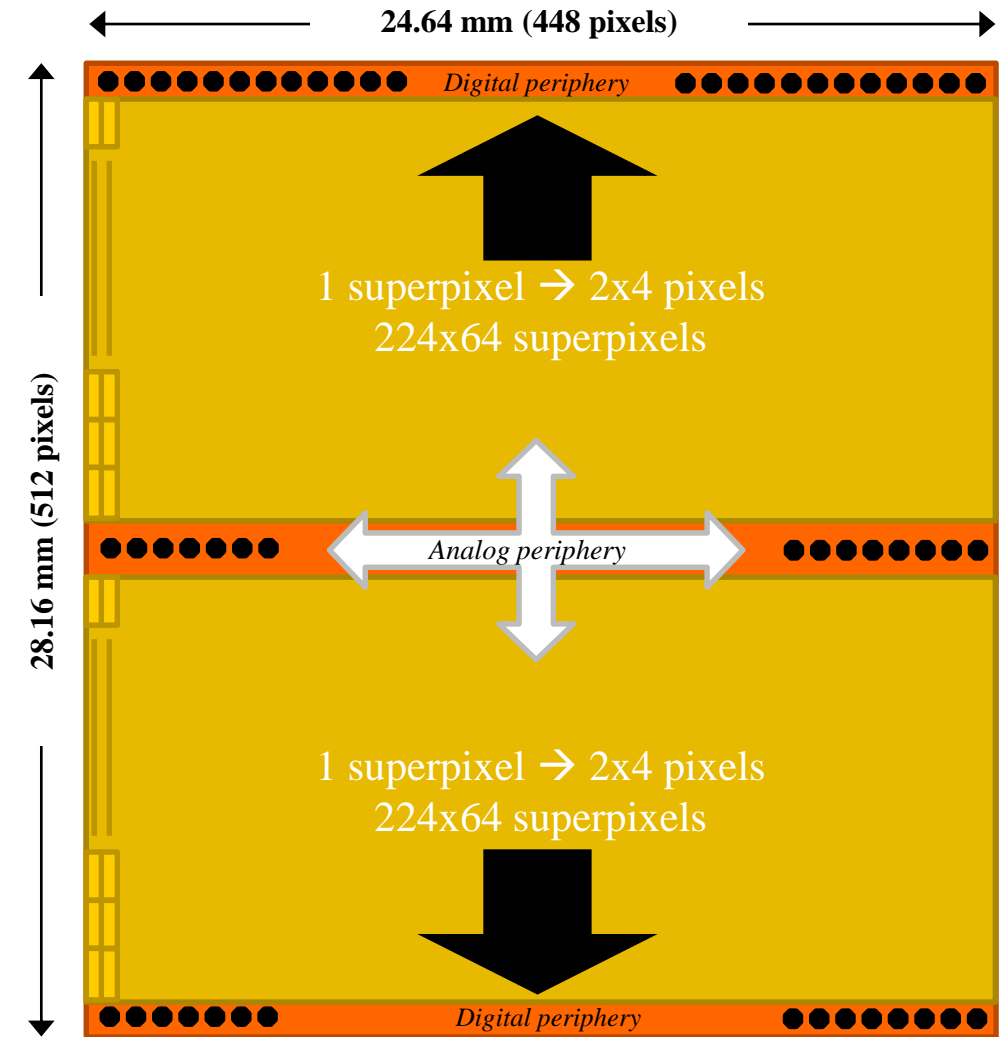


Corrected by field shaping wires
(from UV laser measurement)



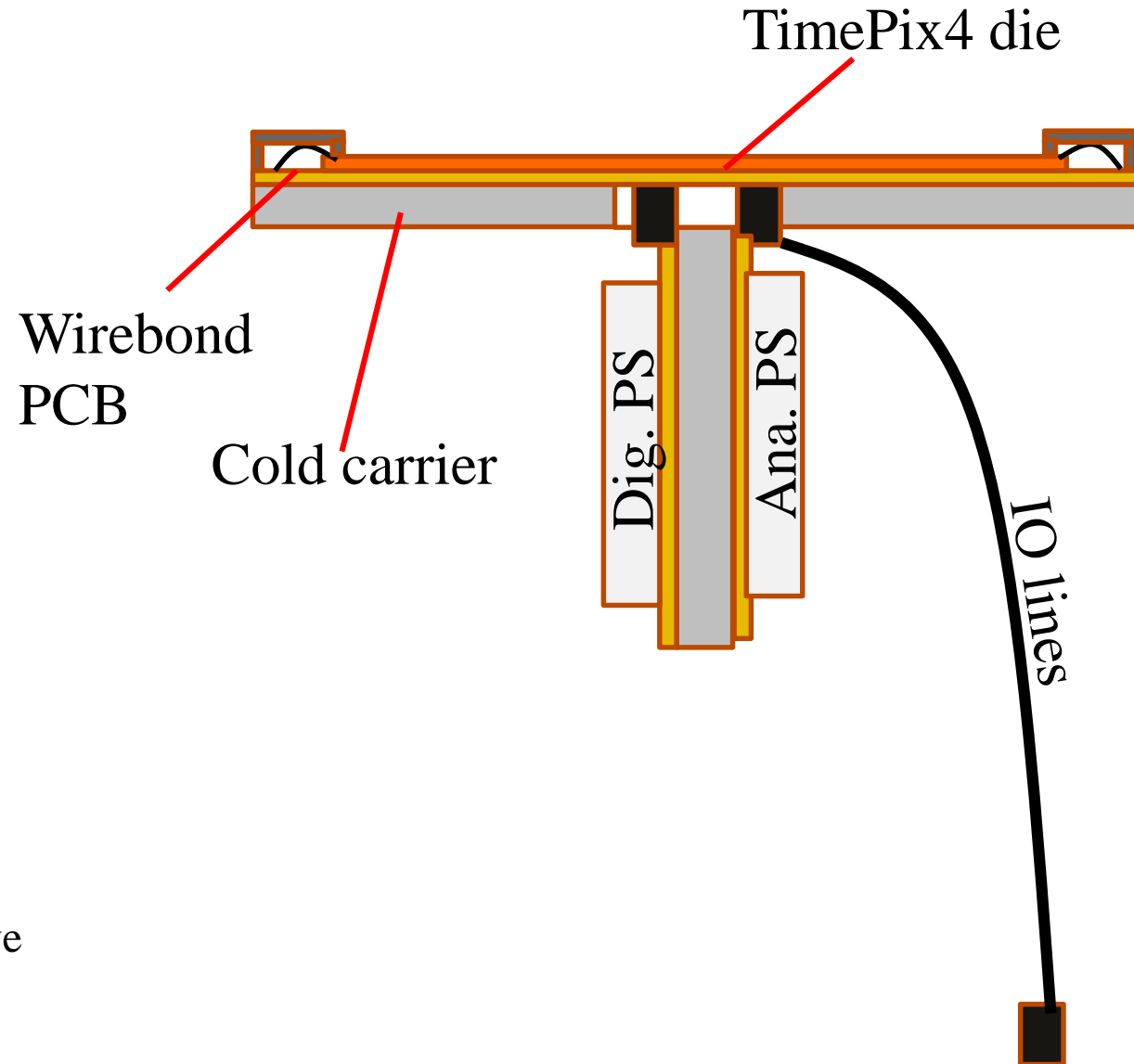
Future development: TimePix4

- Much larger die => 3.5 x active surface of TimePix3
- Same pixel pitch as TPX3 (55 x 55 μm)
- Electronic peripheries also covered with active pixels
- 8 x higher RO speed than TPX3
 - 357.7 vs 45 Mhits/cm²
- No multiplexing electronics needed
 - Chips may be daisy chained
- Just submitted, first (diced) chips expected end January 2020



Suggested GridPix building block based on TPX4

- Detector unit based on a single TPX4
 - Comparable with TPX3 quad
 - Design still at a very preliminary stage
- Much less wire bond pads
 - ~ 100 vs 368
- Larger wirebond pitch
 - 168 vs 73/146 μm
- \Rightarrow wirebond PCB might be much cheaper
- Better continuous tracking
 - ~ 45% less boundaries than in TPX3 quad
- Active surface for wirebond version > 73% (68.9% for quad)
- Possibly in future Through Silicon Via (TSV) connections will be realized \Rightarrow active area > 90%



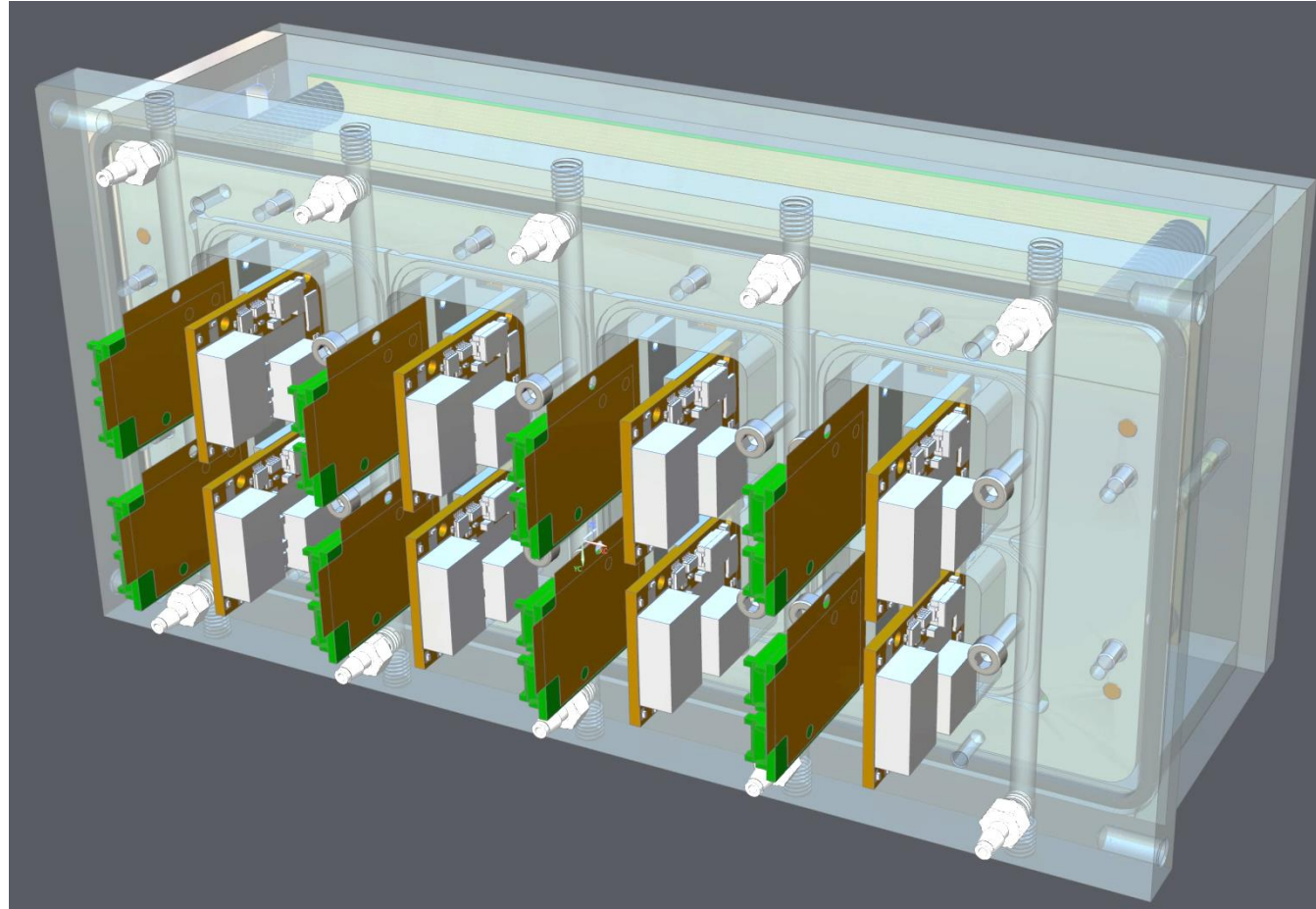
Summary

- A module containing 8 quads, covering about 90 cm² has been realized
 - 62 cm² of the surface is active
- Many performance tests have been done with ionization tracks created by a UV laser to find optimal HV settings
- Systematic errors on tracks at the edge of the TPX3 chips can be significantly reduced by using guard wires
- In future a GridPix unit using a TPX4 chip will increase the sensitive area, reduce the length of the boundaries and reduce the costs

SPARE

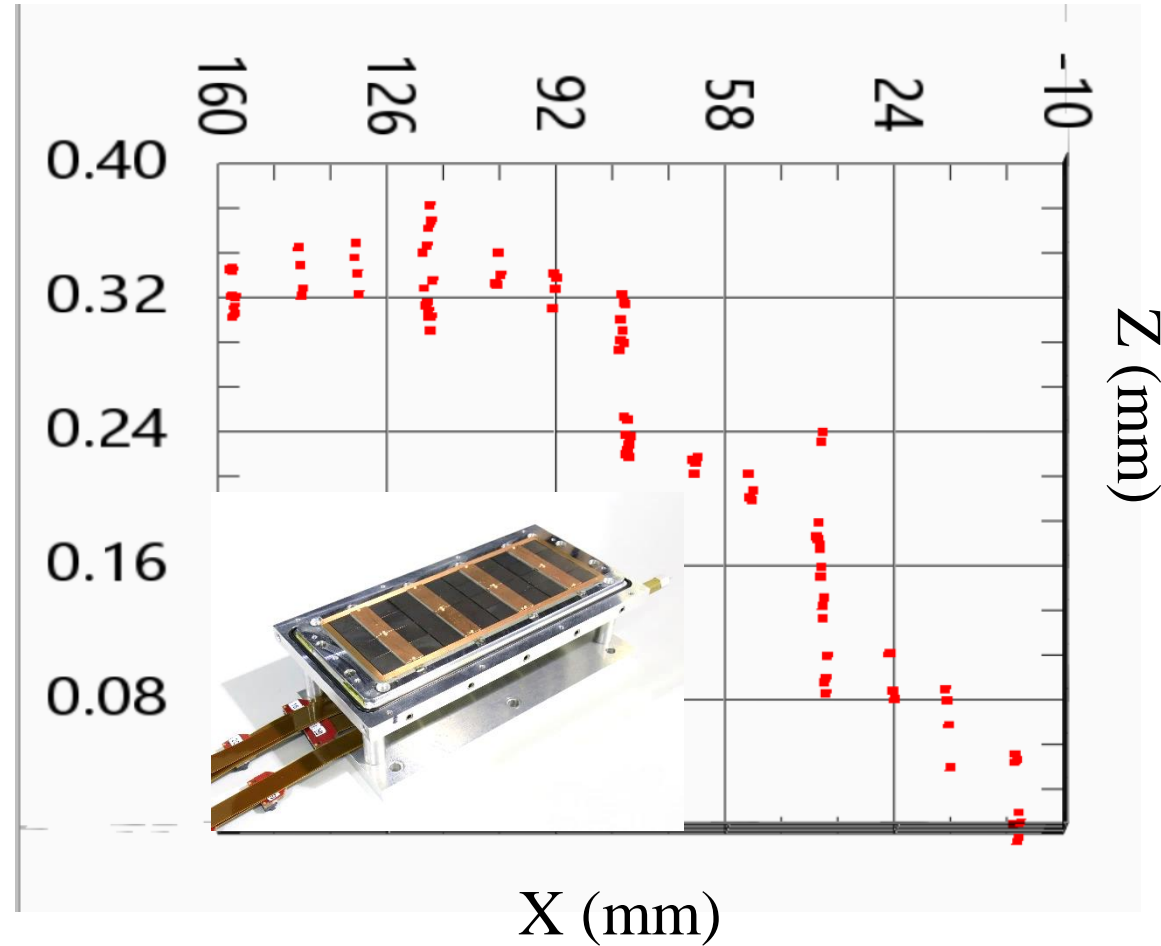
New test box design

- Liquid cooling by drilled channels, connected by silicon tubing
 - Most reliable in this stage of prototyping



Metrology

- XYZ measurement in two steps across the full length and width
- Base plate very bad flatness
 - More than 300 μm
- Corresponds with variations in thickness of the plate
 - \Rightarrow underside may be well flat
- Some torsion in Y
 - Two chips tilted
 - 100 and 150 μm



Preliminary height check

- Two chips were tilted ($\sim 250\text{ }\mu\text{m}$)
- Caused by slanting cutting edge of certain chips

