

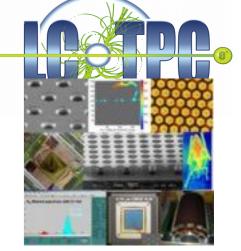
# Status Hardware development of SRS-based readout of Timepix3 at Bonn

2.7.2018 Bonn-Nikhef Meeting



### Scalable Readout System

A generic readout system for laboratory and detector instrumentation developed and supported by the RD51 collaboration.



Common platform for detector readout for gaseous detector Community.

About 80 Systems of various sizes sold.

Different ASICs implemented: APV25, VFAT, Beetle, Timepix - VMM, Timepix3

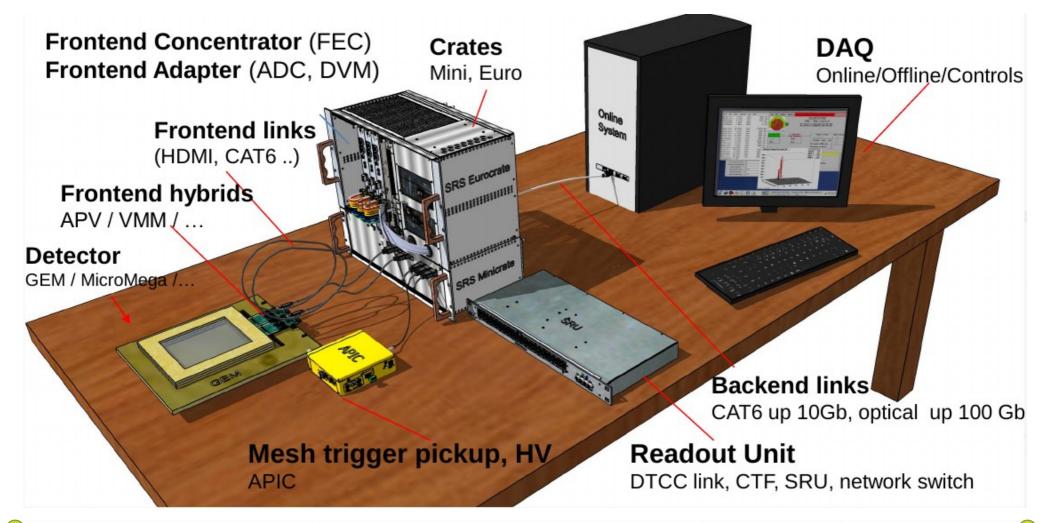
#### Principle ideas:

- · Important (and expensive) hardware components can be reused only some PCBs and the FPGA code have to be redesigned
  - → fast changes between ASICs is possible
- · Easy scaling from a few dozens of channels to tens of thousands
- · Collaboration wide development
- · Open source of codes and designs.



## **Scalable Readout System**

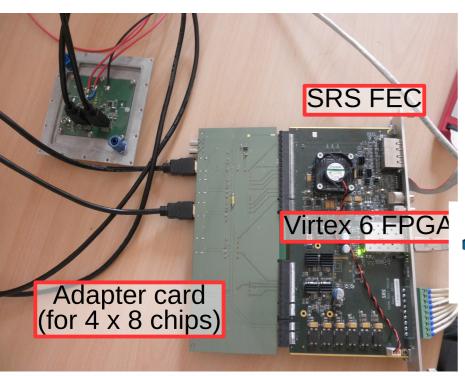


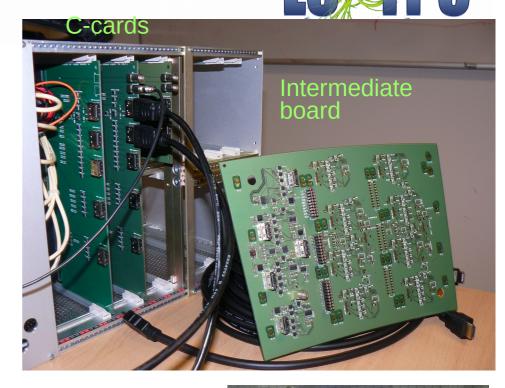


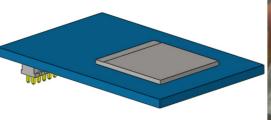


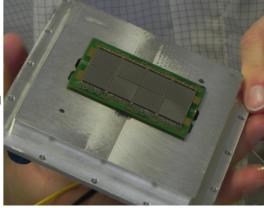
#### **Readout of Timepix**

- Developed by M. Lupberger
   A- or C-card as adapter for FEC
   Intermediate board
- Single Chip Carrier or OctoboardsFPGA code TOF
- Data acquisition program TOS











#### **Readout of Timepix3**



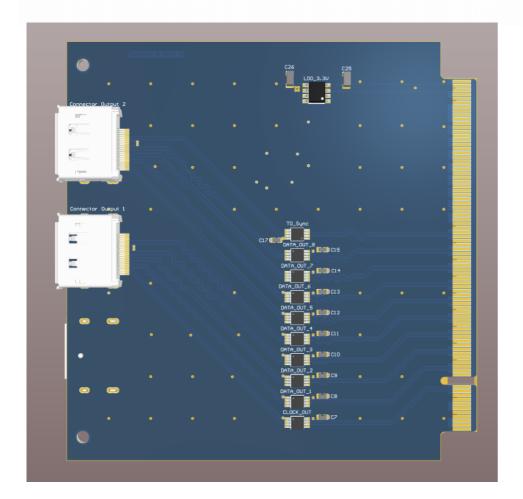
Hardware layout similar to the hardware of Timepix readout:

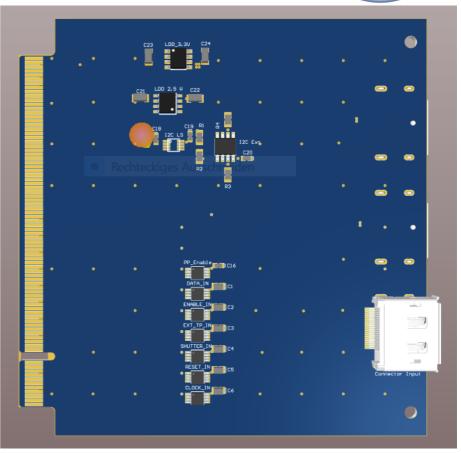
- Smaller A-type adapter card:
  - Mostly an adapter from VME connector to displayport connector, holds also drivers.
  - Appropriate to read out 1 Timepix3 with all 8 LVDS lines or 8 Timepix3 with one line each
- Displayport cables connect to
- Intermediate Board: Connectors for displayport cables and LV supplies.
   Later versions are planned to hold DACs for external test pulses, ADCs for analog level testing etc.
- Direct connection (pin header) or short cables O(10 cm) to
- Chip Carrier with 1 8 Timepix3 ASICs



# **Status of Adapter Card**





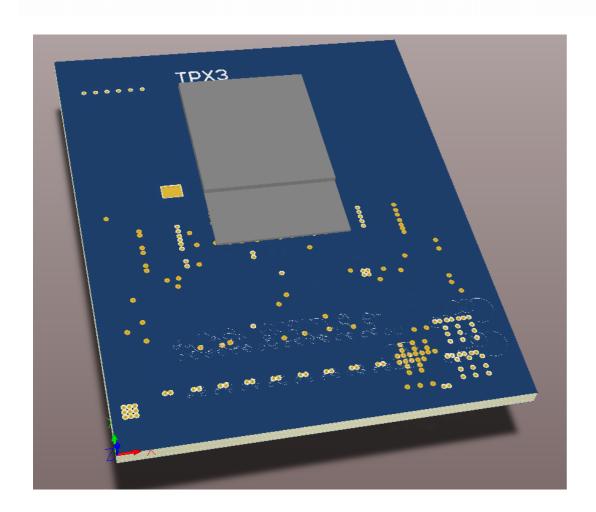


Design has finished.



### **Status Chip Carrier**





Design finished by T. Schiffer.

Intermediate Board:
Currently the design has started. Once the complete chain is availble, the boards will be produced and tested.

Software is currently being developed on a Virtex6 evaluation board (s. presentation by M. Gruber).

