Timepix3 SRS readout

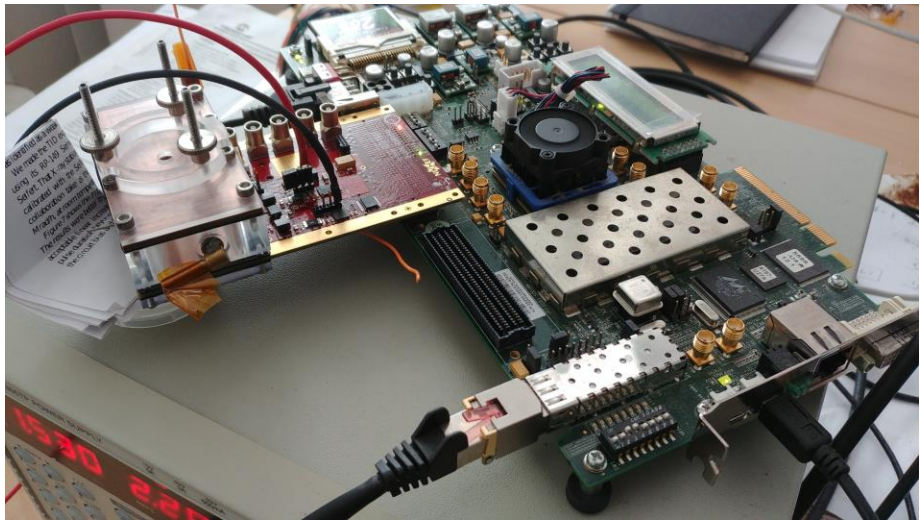
SOFTWARE STATUS

Basics of implementation

- Implementation in Python with usage of Basil framework (https://github.com/SiLab-Bonn/basil)
- GNU General Public License v3.0
- Testing in interpreter mode – will be compiled for operation
- Including interfaces for event display, monitoring and online analysis
- Separate “class” for each chip based on its ChipID – storage of all configurations (DACs, PCRs, …) chip wise

Testing setup

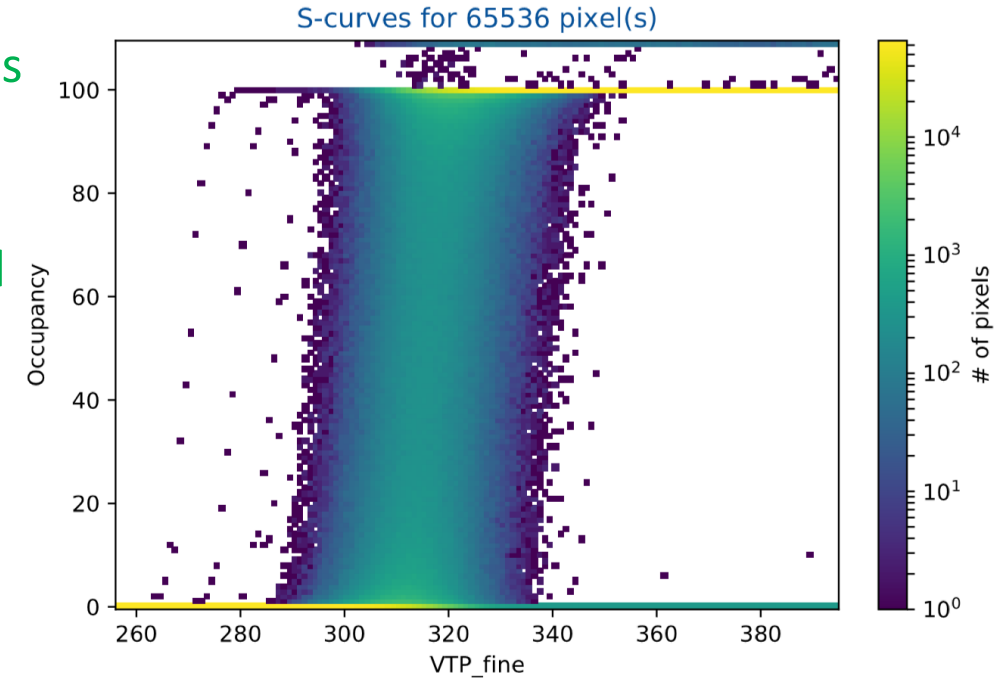
- Nikef Timepix3 carrier
- Virtex6 Evaluation Board (ML605)
- Usage of 1 active output channel
- Readout clock (DualEdge on): 160 MHz
- Firmware transmits binary commands for the Timepix3 and does 10b to 8b decoding



Current status

Done:

- Reading and writing all registers (DACs, TPs, Config, PCR, …)
- Setting chip up with configurations defined by YAML files
- Reading pixel data (PCR, CTPR, Measured Data) in sequential and in Data driven mode
- Appling test pulses and reading the produced data
- S-Curve scan based on a generic scan script
- Storing of raw data and PCR in HDF5 files



Current status

Work in progress:

- Additional scans (Equalisation, ToT calibration)
- Fast and mode dependent data decoding
- Development of unit tests for setting up a CI and for testing new hardware

Planned (near future):

- Recording ^{55}Fe spectrum with a small X-ray detector setup
- Streamlining configurations and data storing for extension to multiple chips